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MS-7529

Version 1.1

CPU:

Intel Conroe (65W Dual core)

System Chipset:

Intel Bearlake - MCH (North Bridge)

Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI

HD -- ALC888

LPC Super I/O -- F71882FG

LAN-- REALTEK RTL8111C Co-lay RTL8101E

CLOCK -- RTM876-665

Main Memory:

DDR II *2 (Max 4GB)

Expansion Slots:

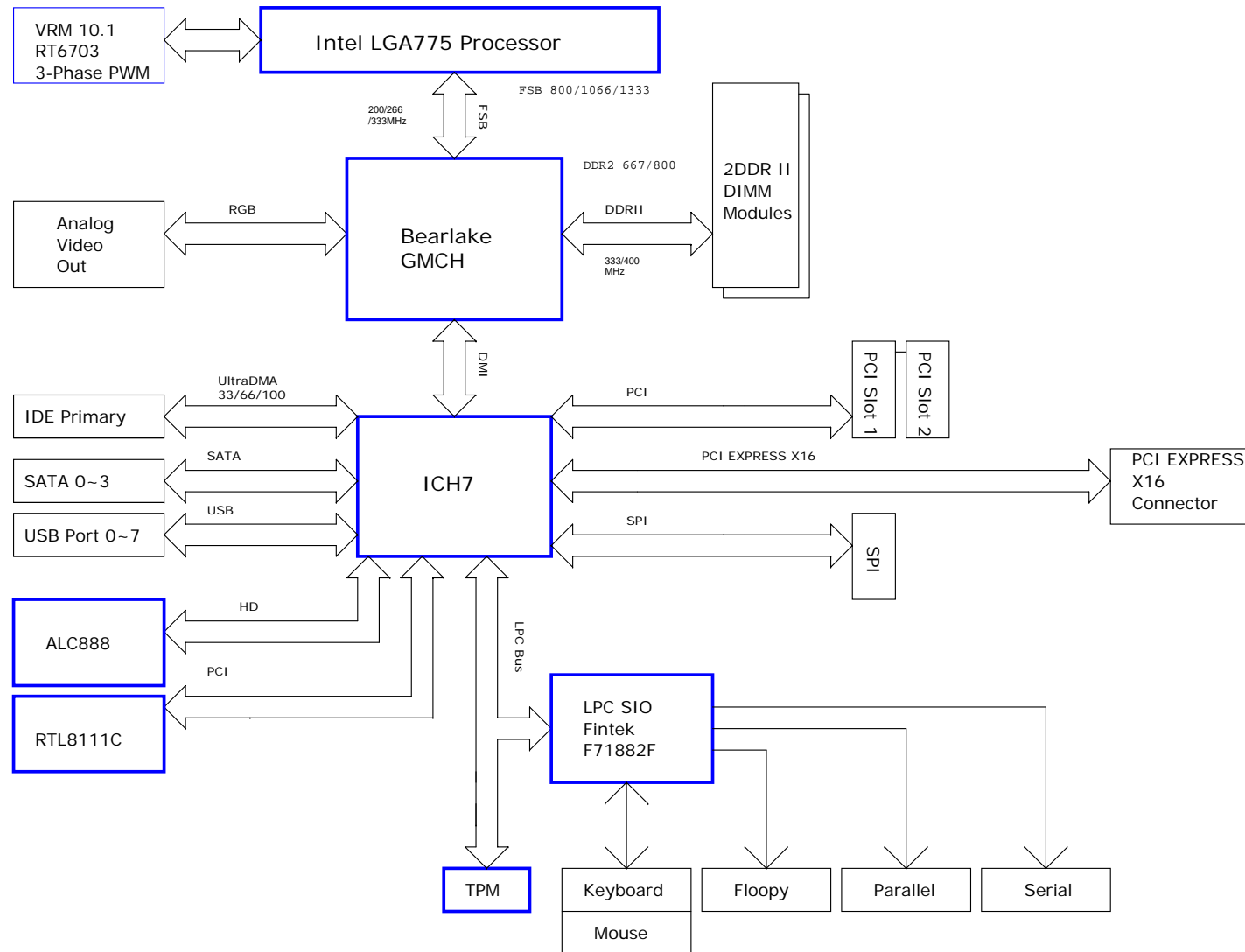
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

Controller: 3 PHASES

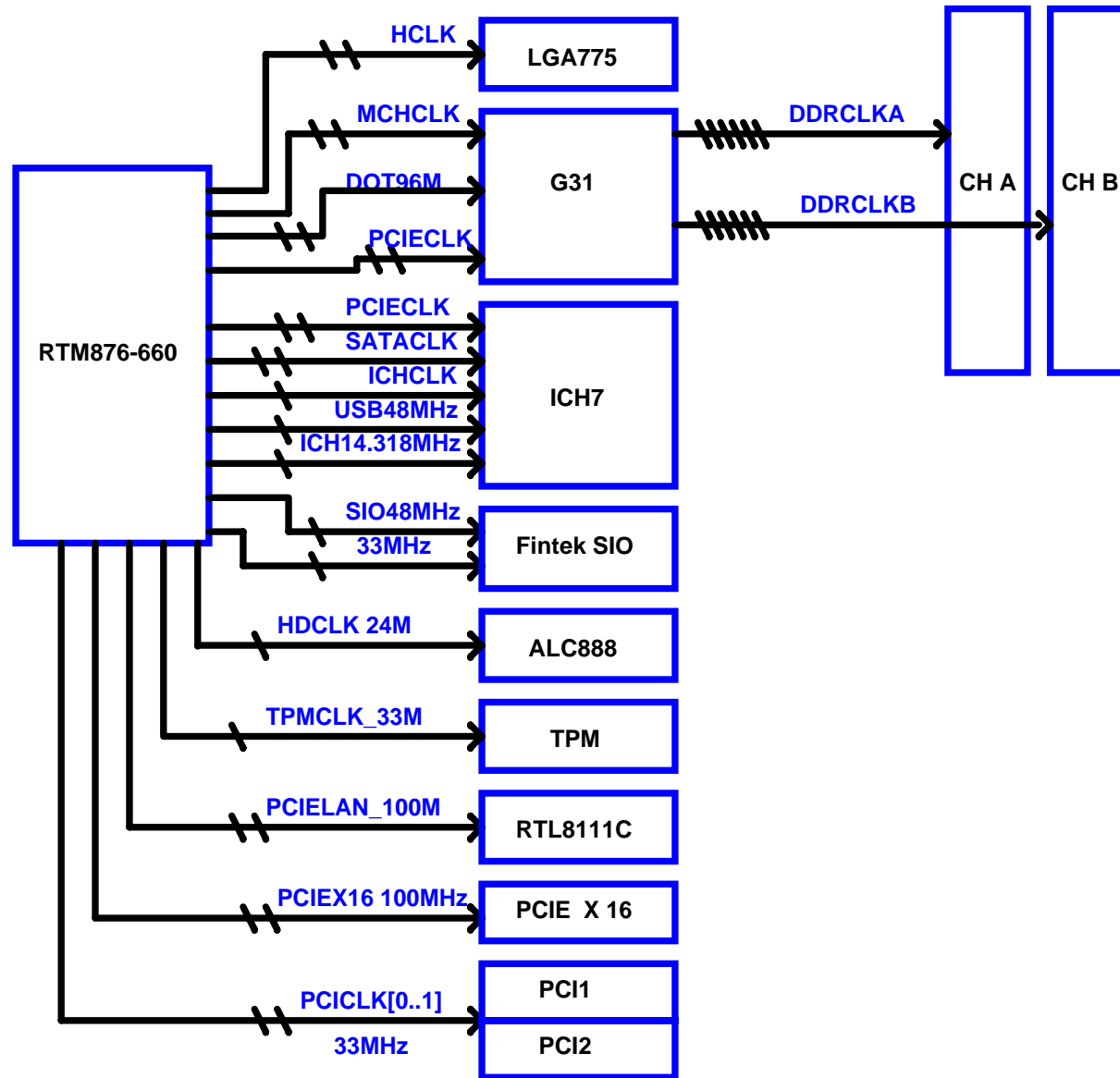
Block Diagram



www.schematic-x.blogspot.com

MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description BLOCK DIAGRAM	Rev 1.1
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CLOCK MAP



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Processor
0.8375-1.6000V Core-125A
1.2V FSB Vtt-5.3A
VCCPLL
VCC-IOPLL & VCCA

G31 MCH
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.5V Core-13.8A(Integrated)
1.5V Core-8.9A(Discrete)
1.5V PCI Express&DMI-1.5A
1.5V PCIE&DMI PLL-45mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
2.5V DAC-70mA*
2.5V HV-3mA
2.5V CMOS-2.0mA

ICH7
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5A*-1.01A
VCC1_5B*-0.77A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-50mA
VccSATAIPLL-50mA

Battery

L6703 Regulator
VCCP
0.8375-1.6000V

VTT Regulator
V_FSB_VTT
1.2V

uP6103 Regulator
VCC_DDR
1.8V

uP6103 Regulator
V_1P5_CORE
1.5V

uP7707 Regulator
V_2P5_MCH
2.5V

1.05V Regulator
V_1P05_CORE
1.05V

uP7706 Regulator
3VSB
3.3V

uP7501 Regulator
5VDIMM
5V

W83310DS Regula
VTT_DDR
0.9V

DDR2 DIMM conn(4) & term
0.9V SM Vtt-1.2A(S0)
1.8V Vdd/vddq-4.7A(S0,S1)

PCIE X16 slot(1)
+12V-5.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCIE X1 slot(1)
+12V-0.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCI slot slot(4)
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-7.6A
+5.0V-5.0A
+12V-0.5A
-12V-0.1A

USB
+5V-4A(S0,S1)

PS2
+5V-345mA(S0,S1)

CLKGEN
+3.3V-560mA

LAN
3VSB-

SIO
+3.3V
3VSB-

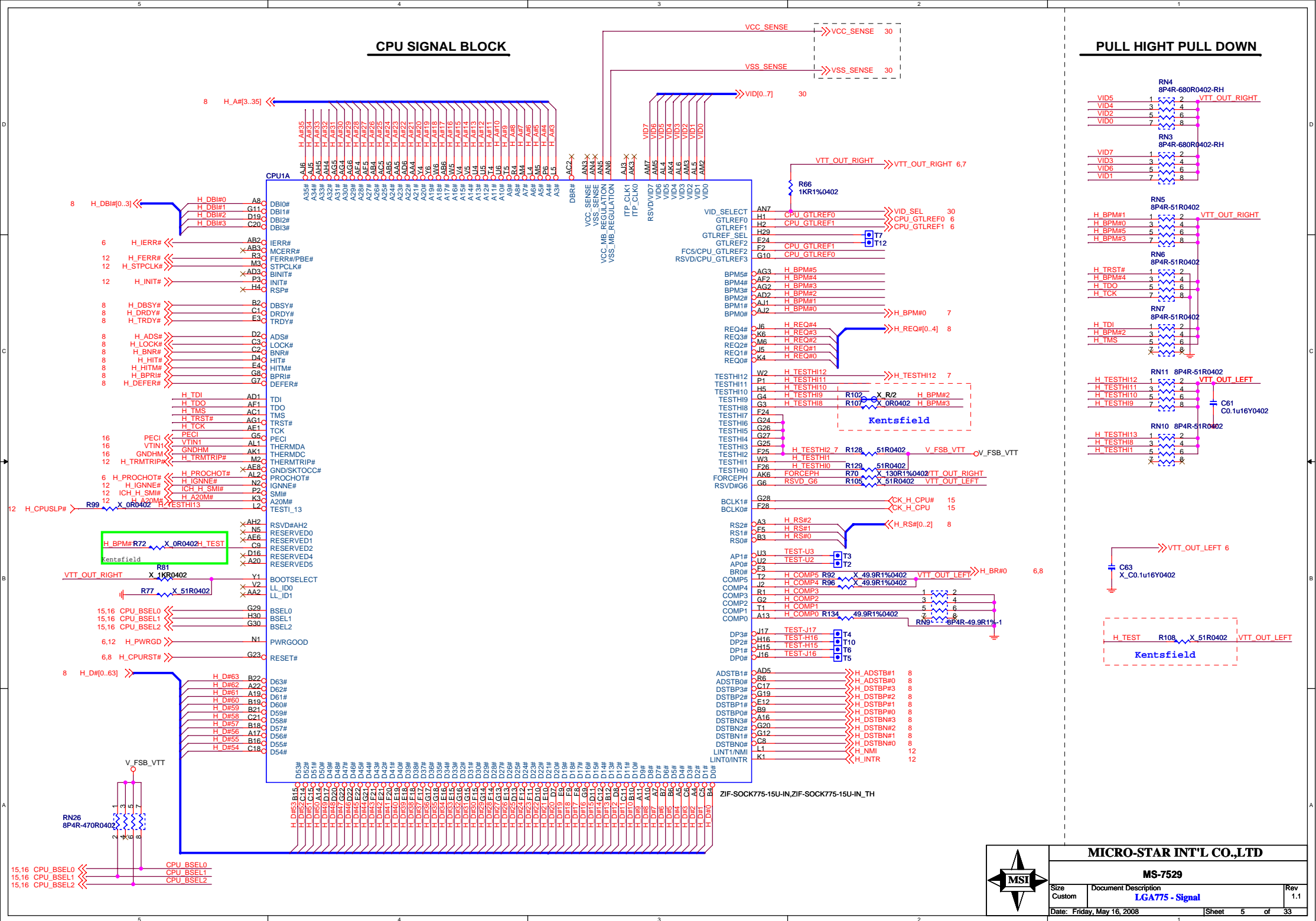
SPI ROM

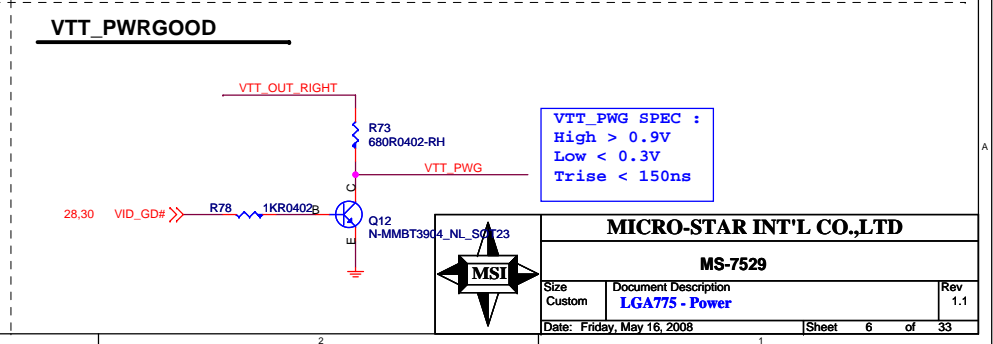
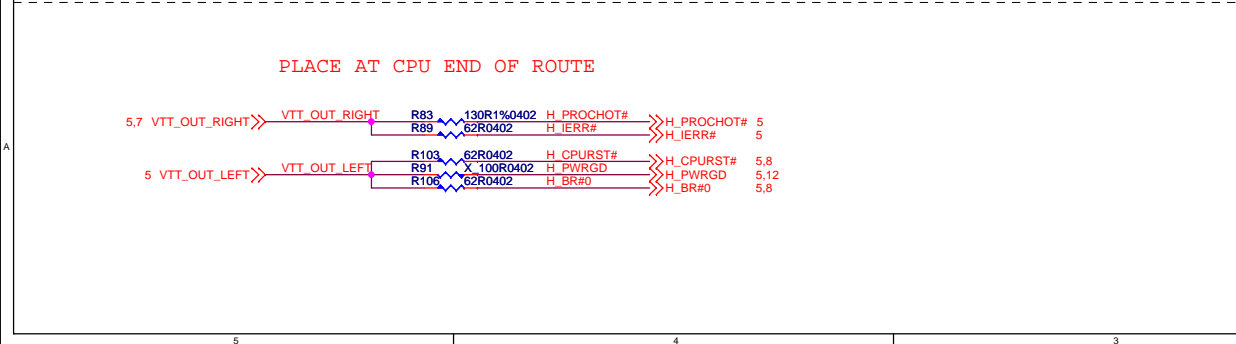
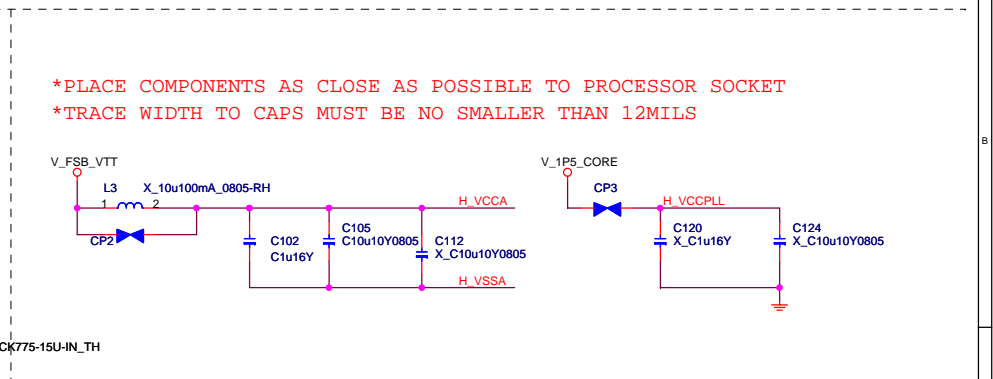
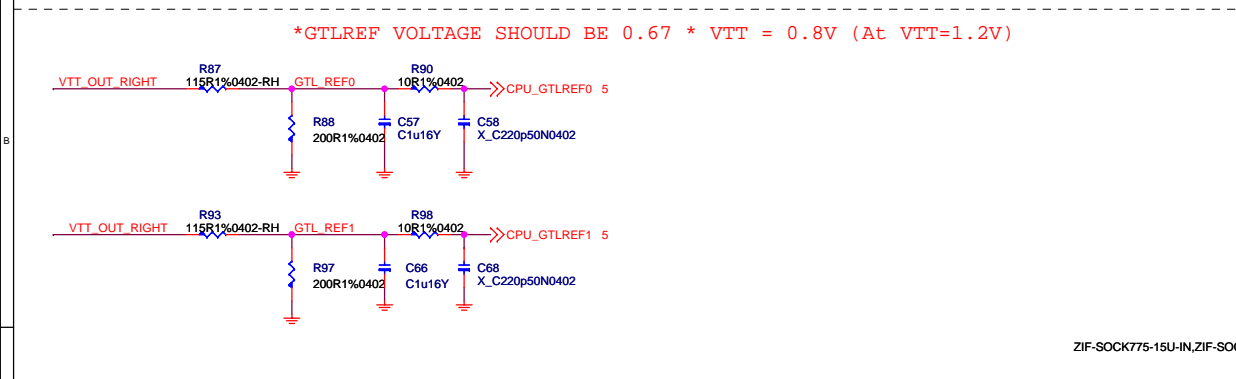
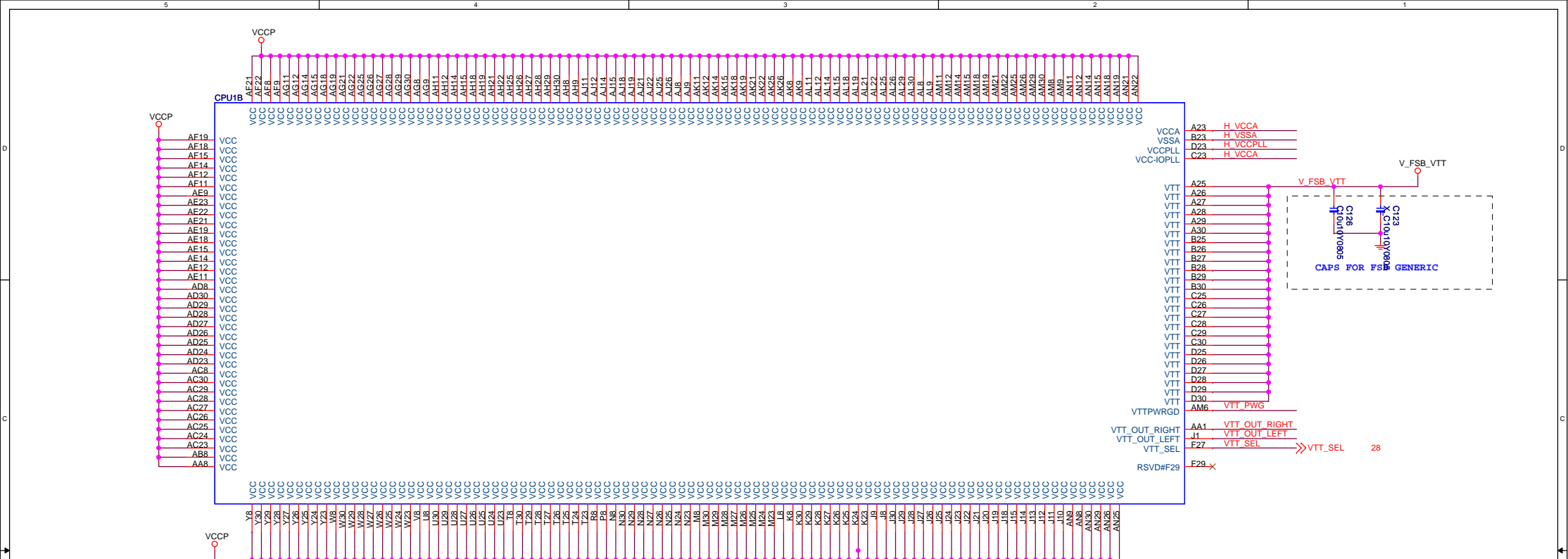
Audio Codec

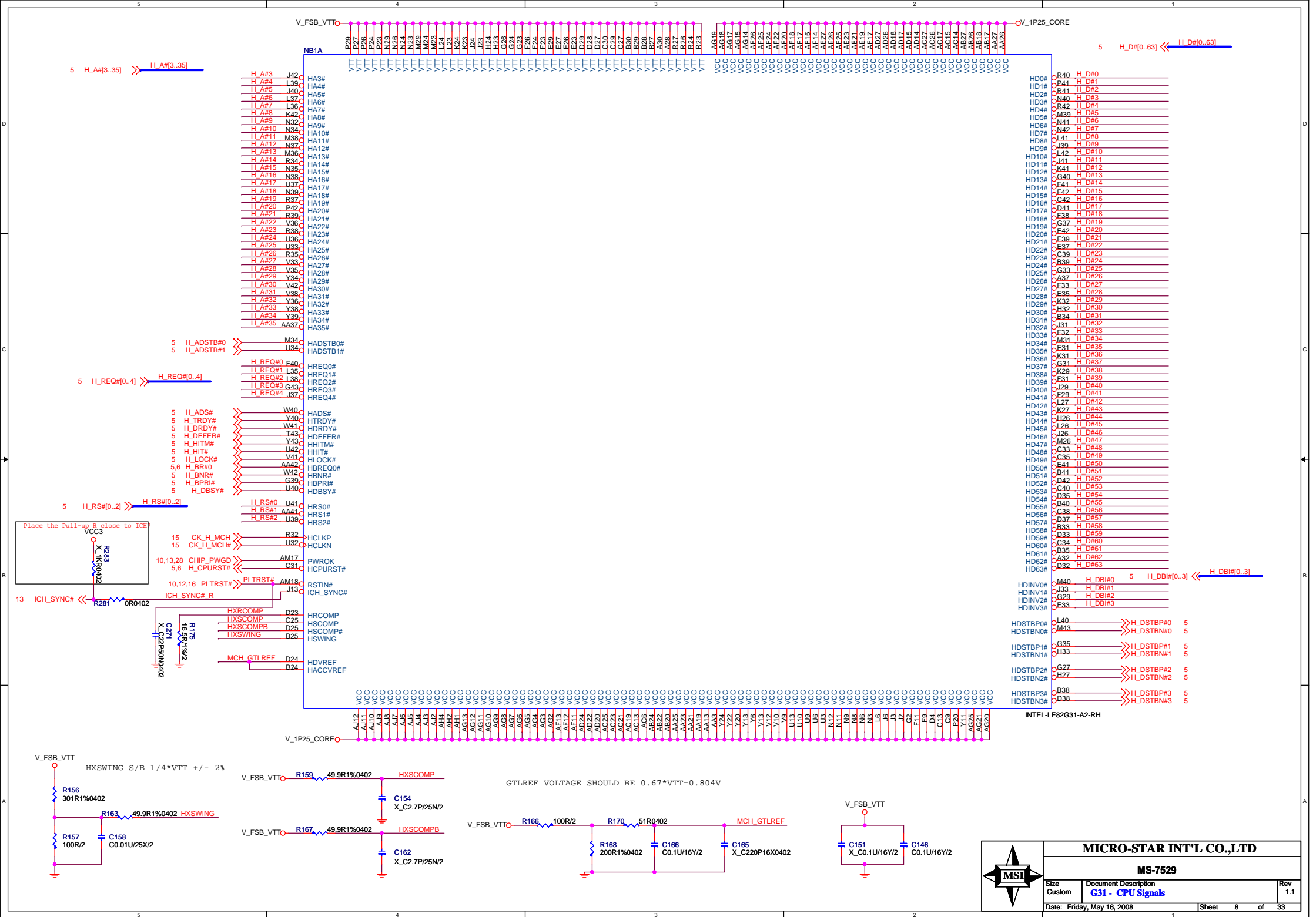
1394

+12V
ATX 2x2

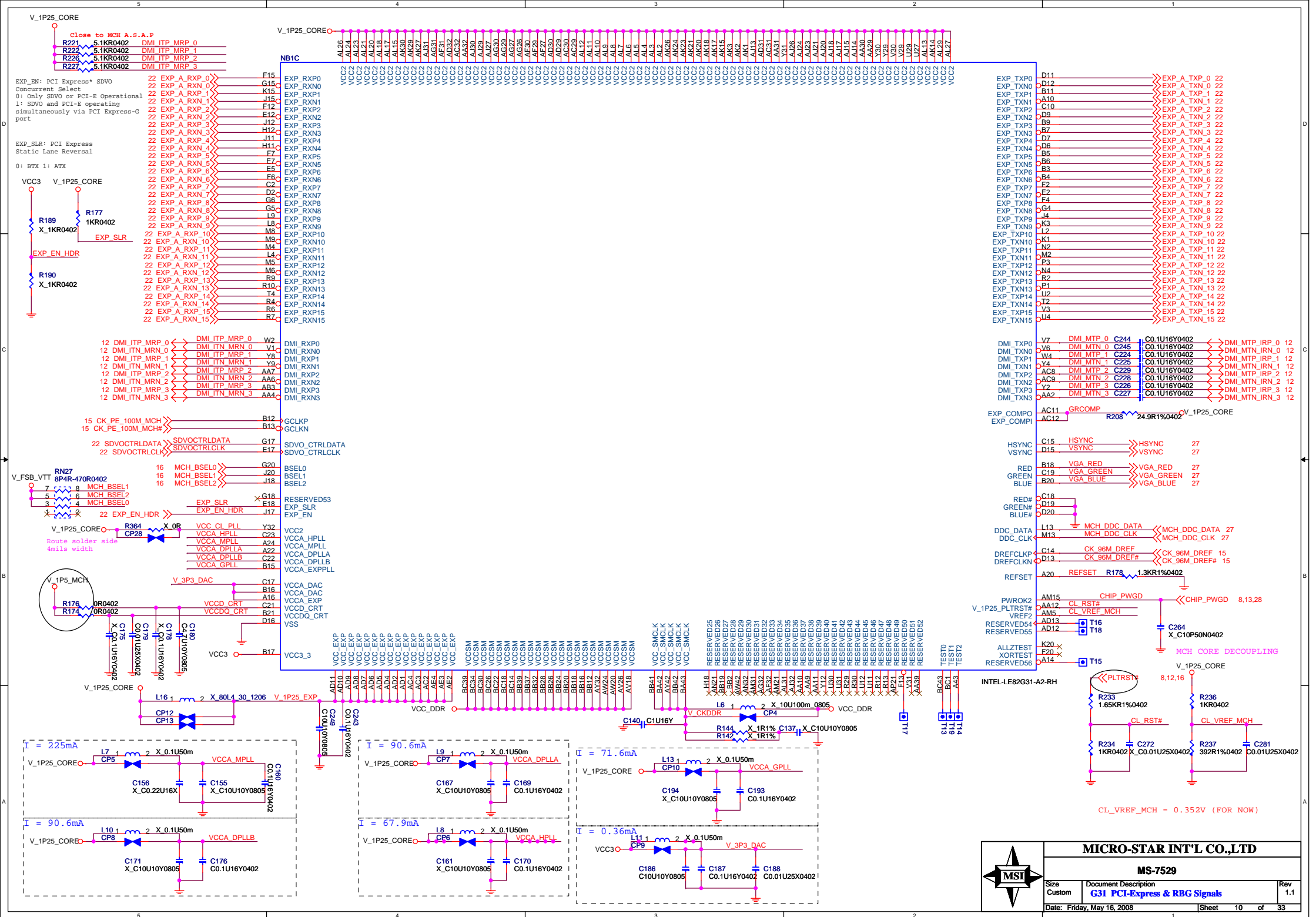
+12V	+5V	+3.3V	+5VSB
ATX POWER			

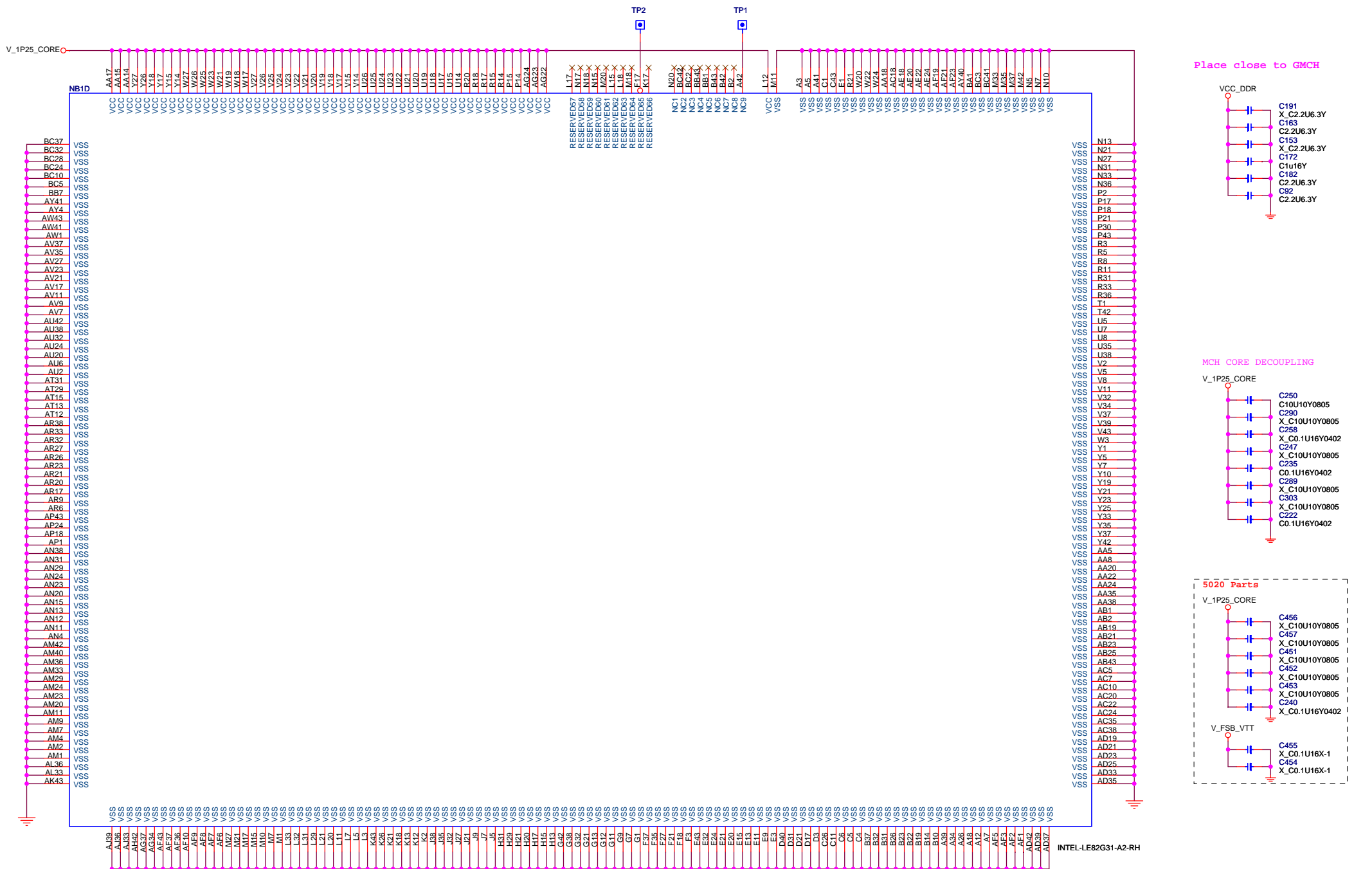




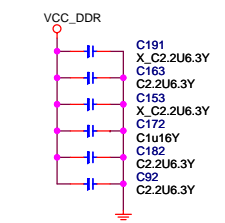




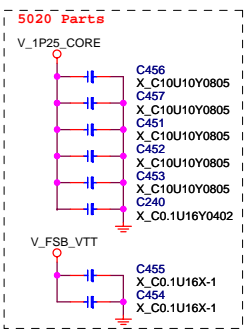
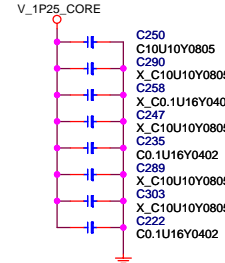




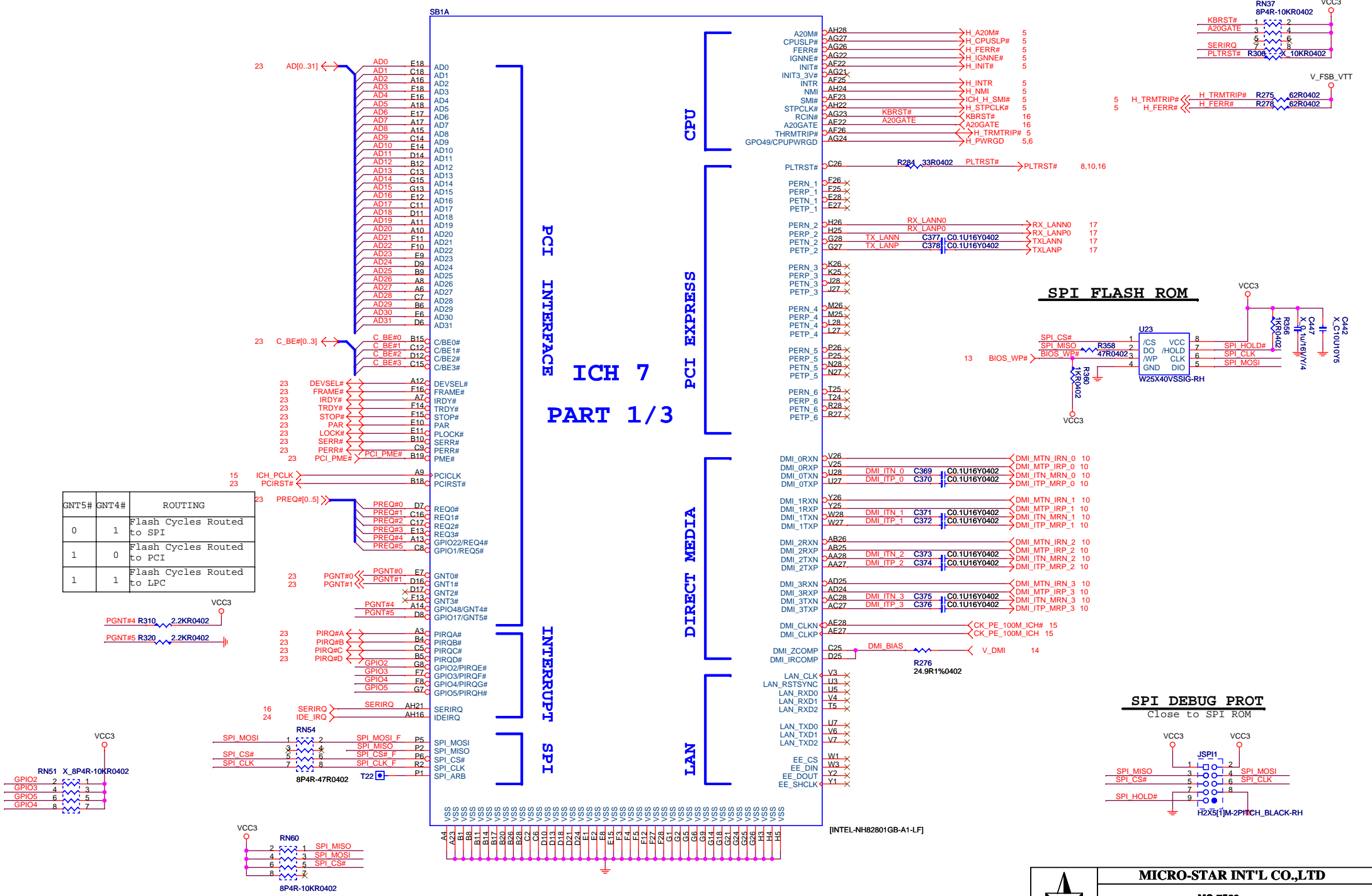
Place close to GMCH



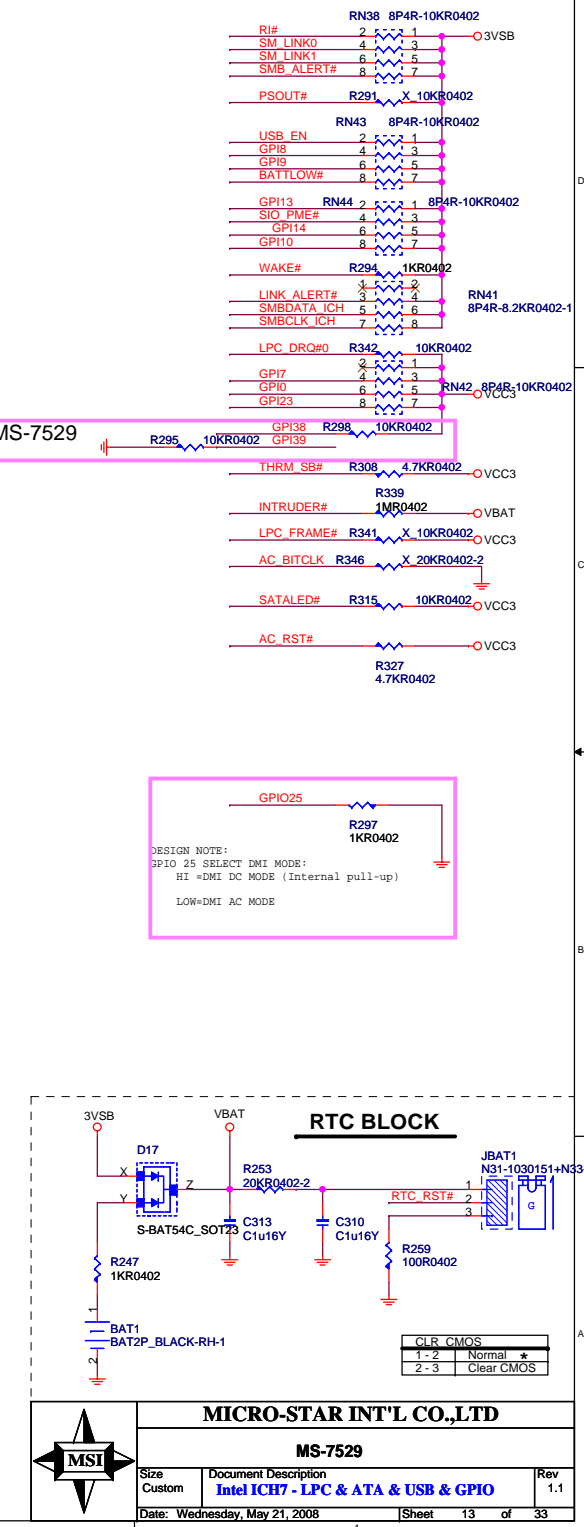
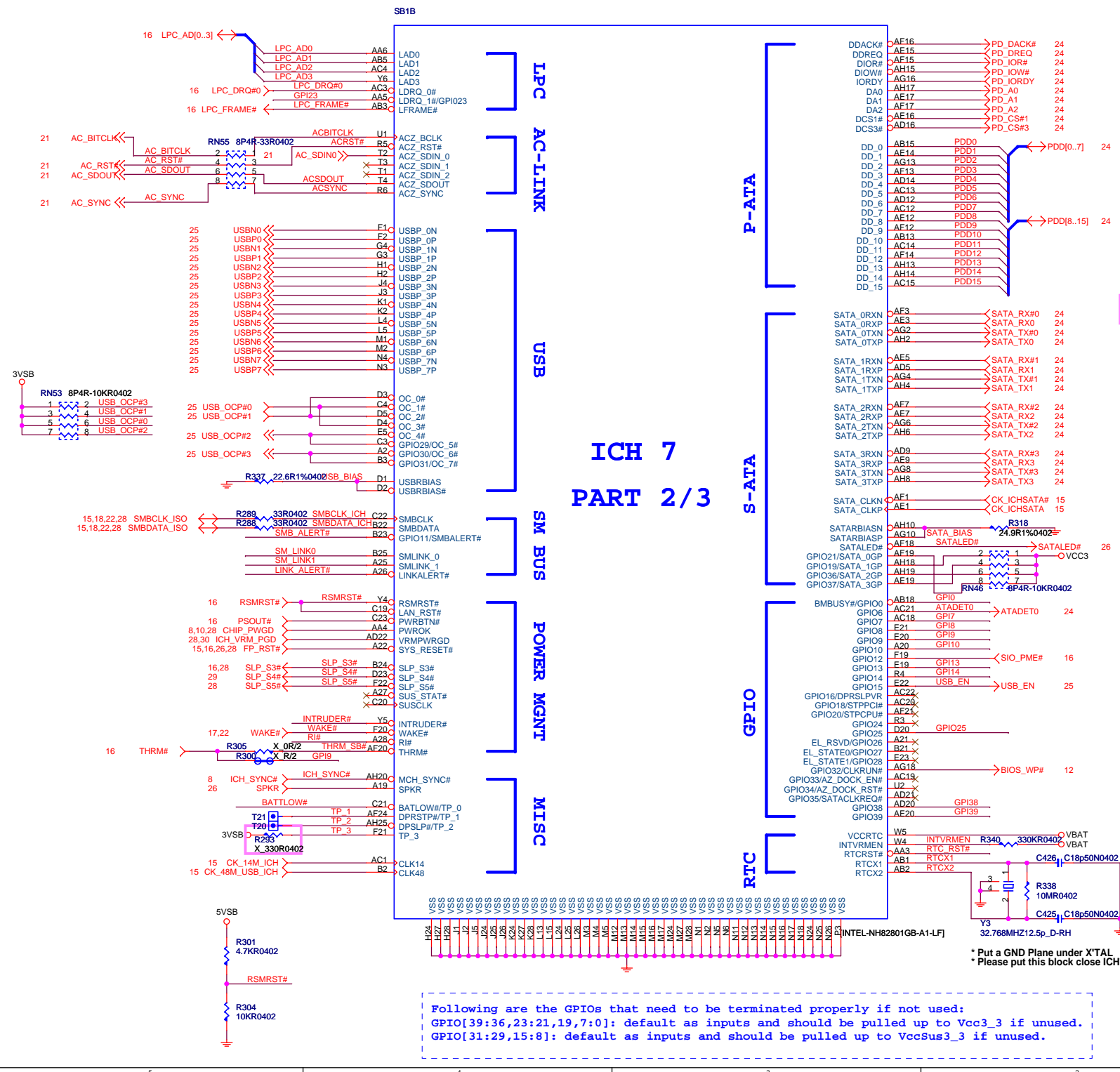
MCH CORE DECOUPLING



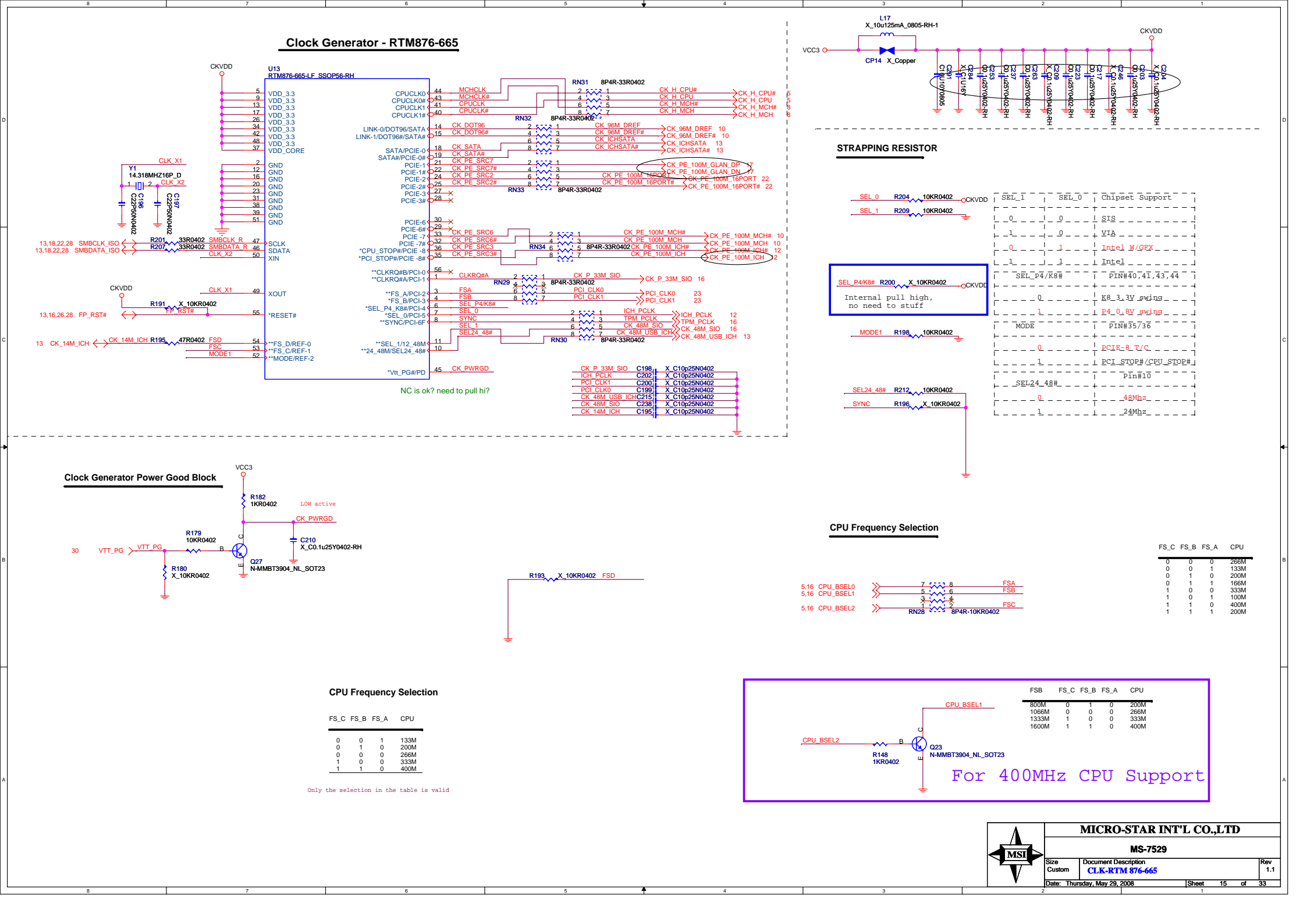
MICRO-STAR INT'L CO.,LTD			
MS-7529			
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GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC





[illegible]

Clock Generator - RTM876-665

Clock Generator Power Good Block

VCC3
R182 1K0R0402 LOW active
CK_PWRGD
C210 X_C0.1u25Y0402-RH
Q27 N-MMBT3904_NL_SOT23
VTT_PG VTT_PG
R179 10KR0402
R180 X_10KR0402
R193 X_10KR0402 FSD

CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid

STRAPPING RESISTOR

SEL_0 R204 10KR0402 CKVDD
SEL_1 R209 10KR0402
SEL_P4/K8# R200 X_10KR0402 CKVDD
Internal pull high, no need to stuff
MODE1 R198 10KR0402
SEL24_48# R212 10KR0402
SYNC R196 X_10KR0402

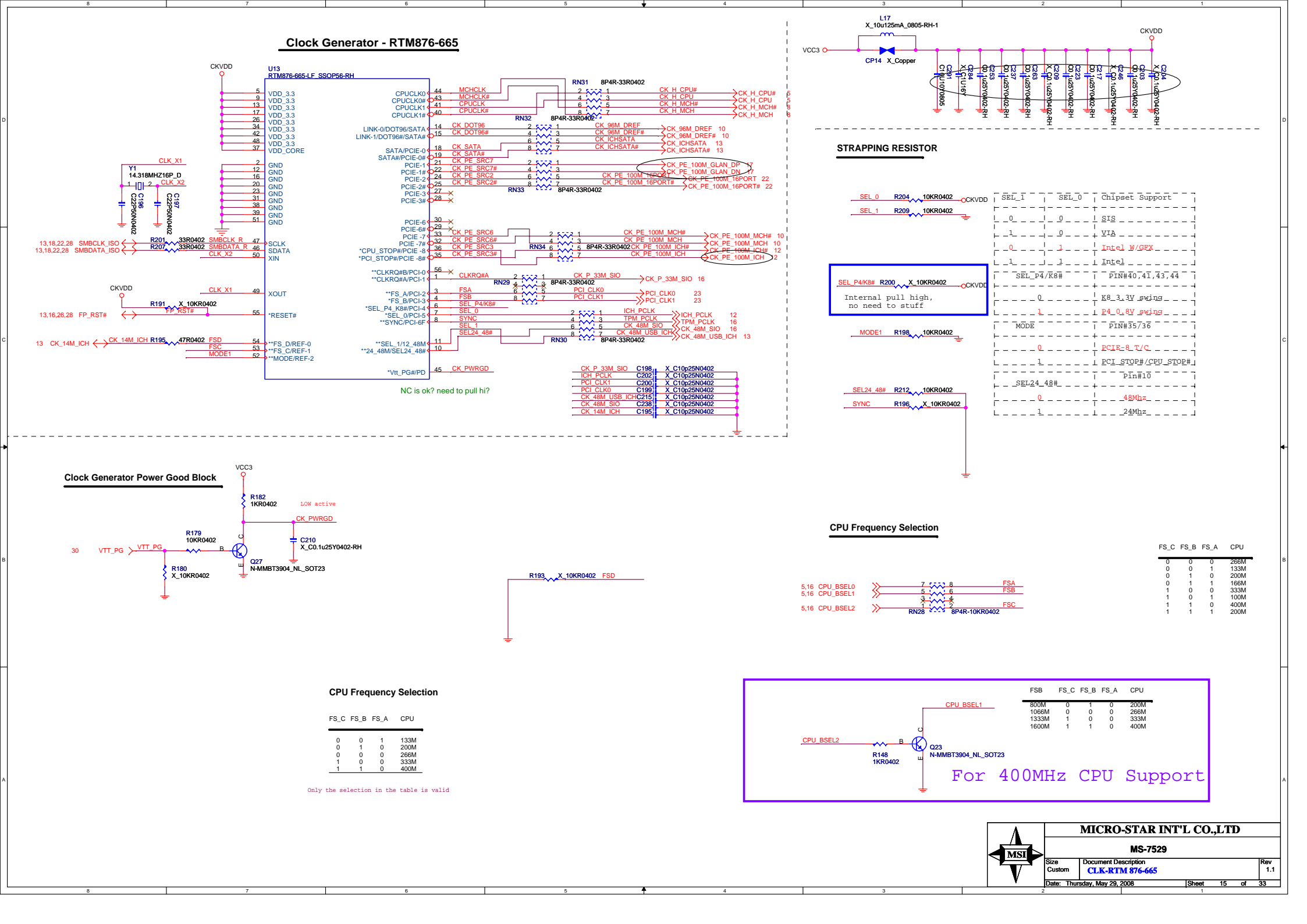
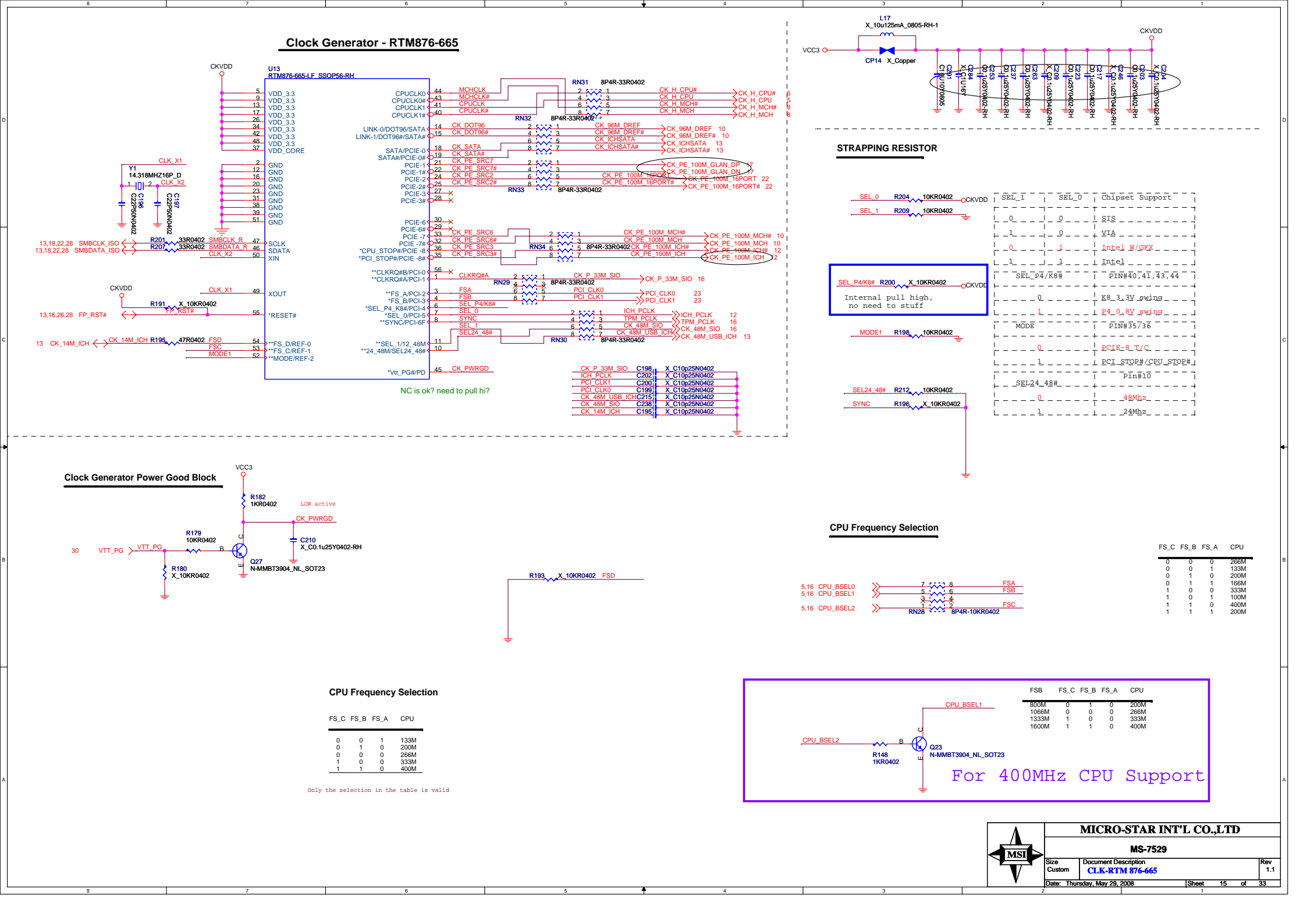
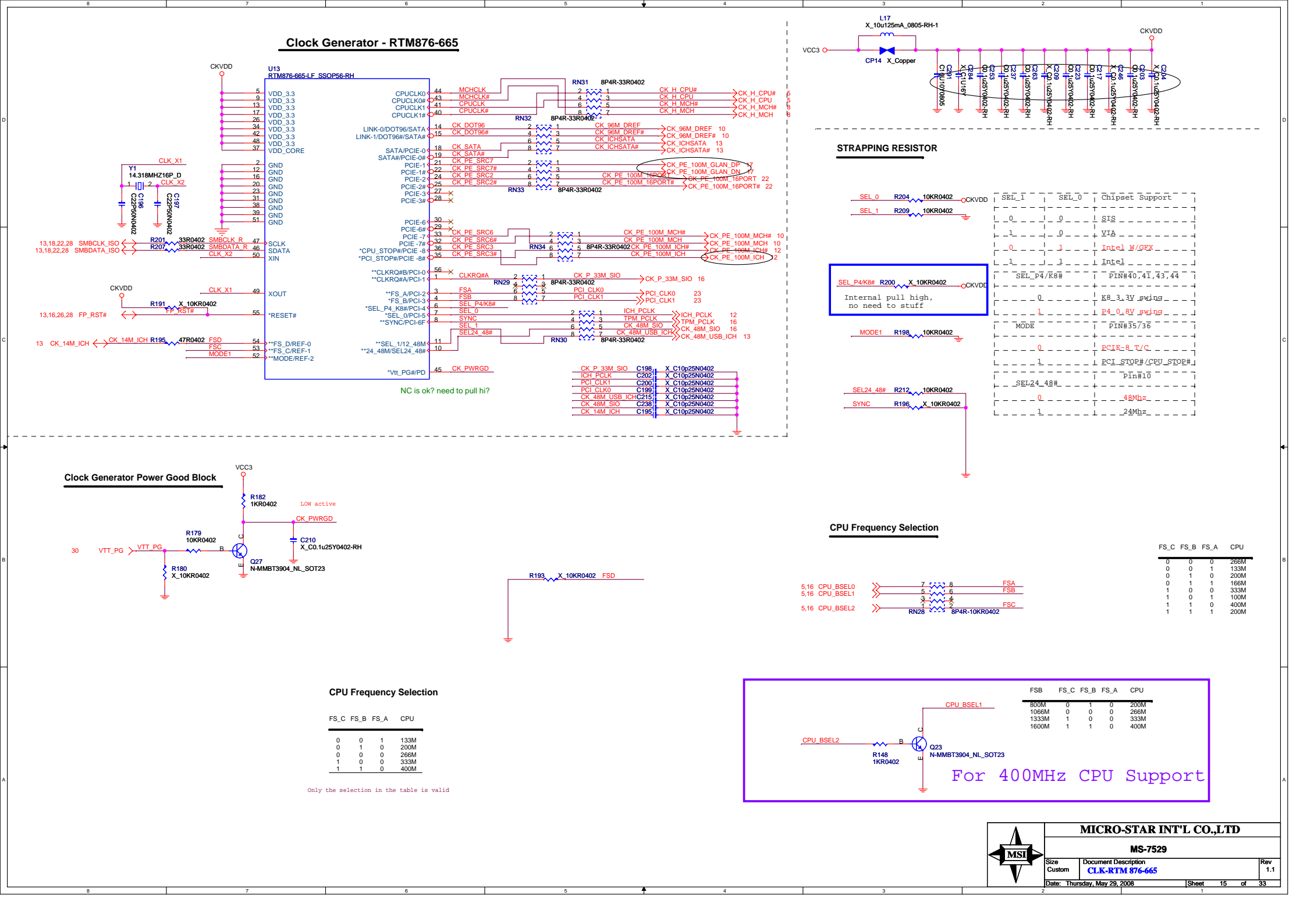
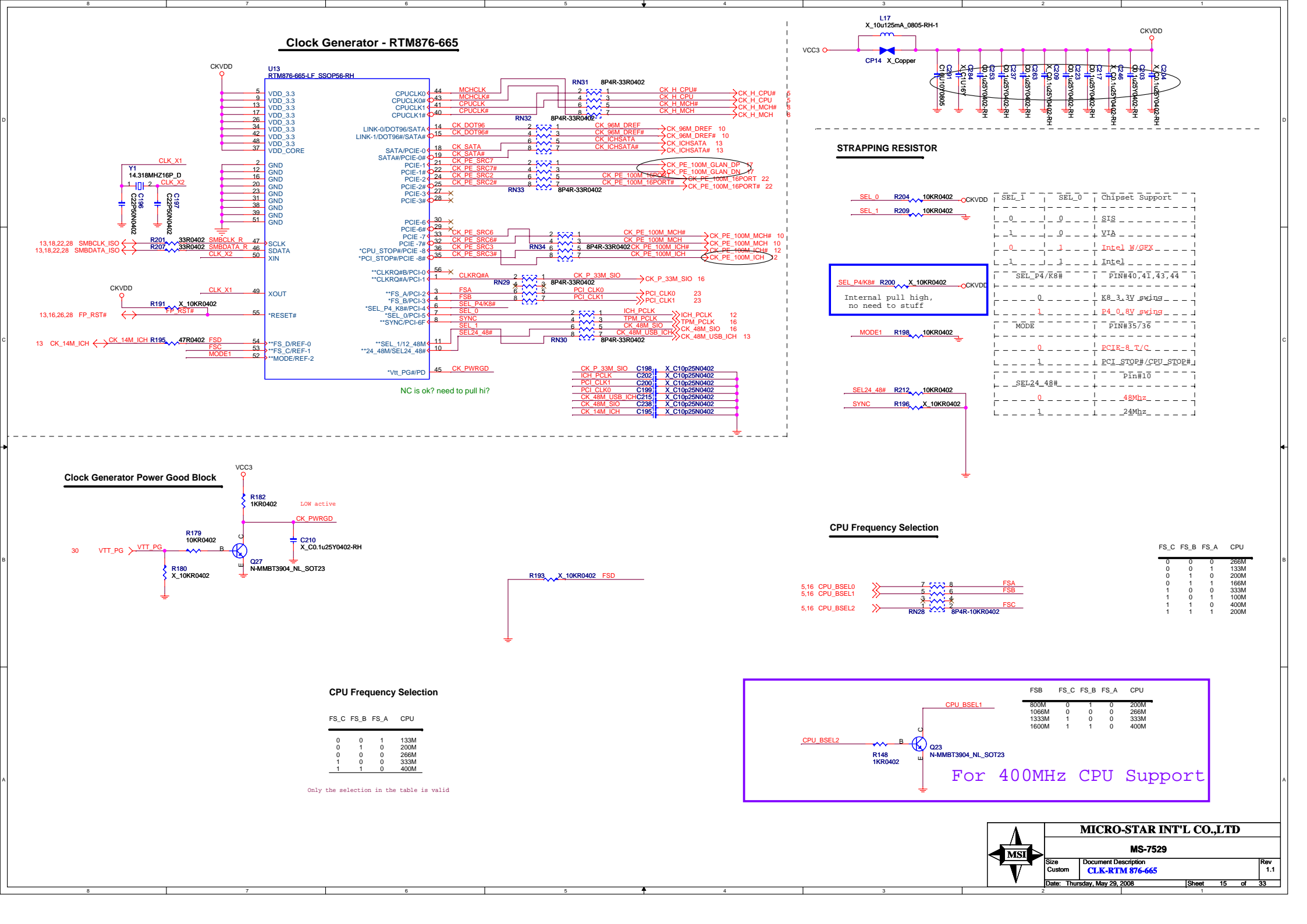
CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

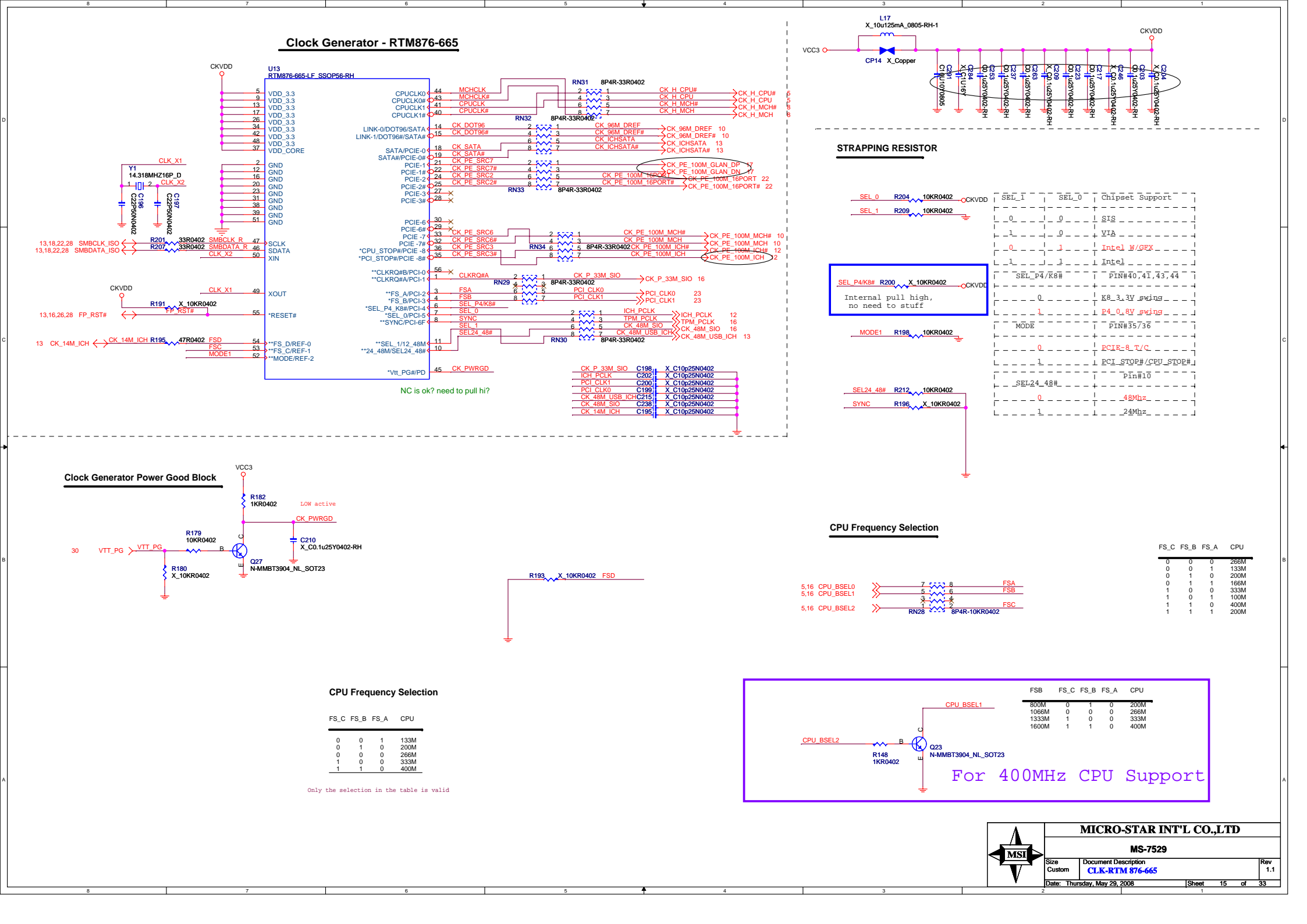
For 400MHz CPU Support

FSC FS_C FS_B FS_A CPU
800M 0 1 0 200M
1066M 0 0 0 266M
1333M 1 0 0 333M
1600M 1 1 0 400M

MSI MICRO-STAR INT'L CO.,LTD MS-7529
Size Custom Document Description CLK-RTM 876-665 Rev 1.1
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Clock Generator - RTM876-665

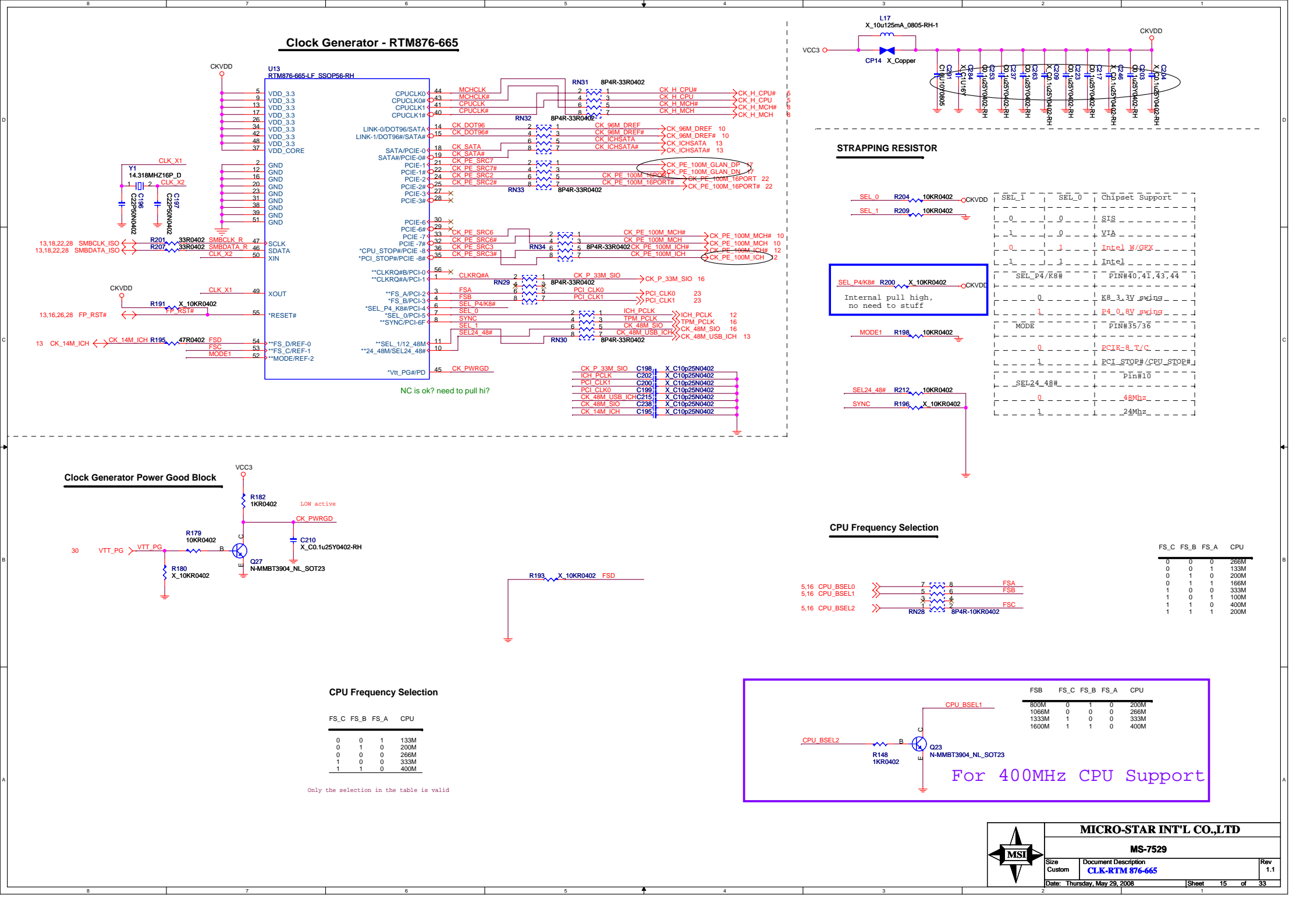


Clock Generator - RTM876-665

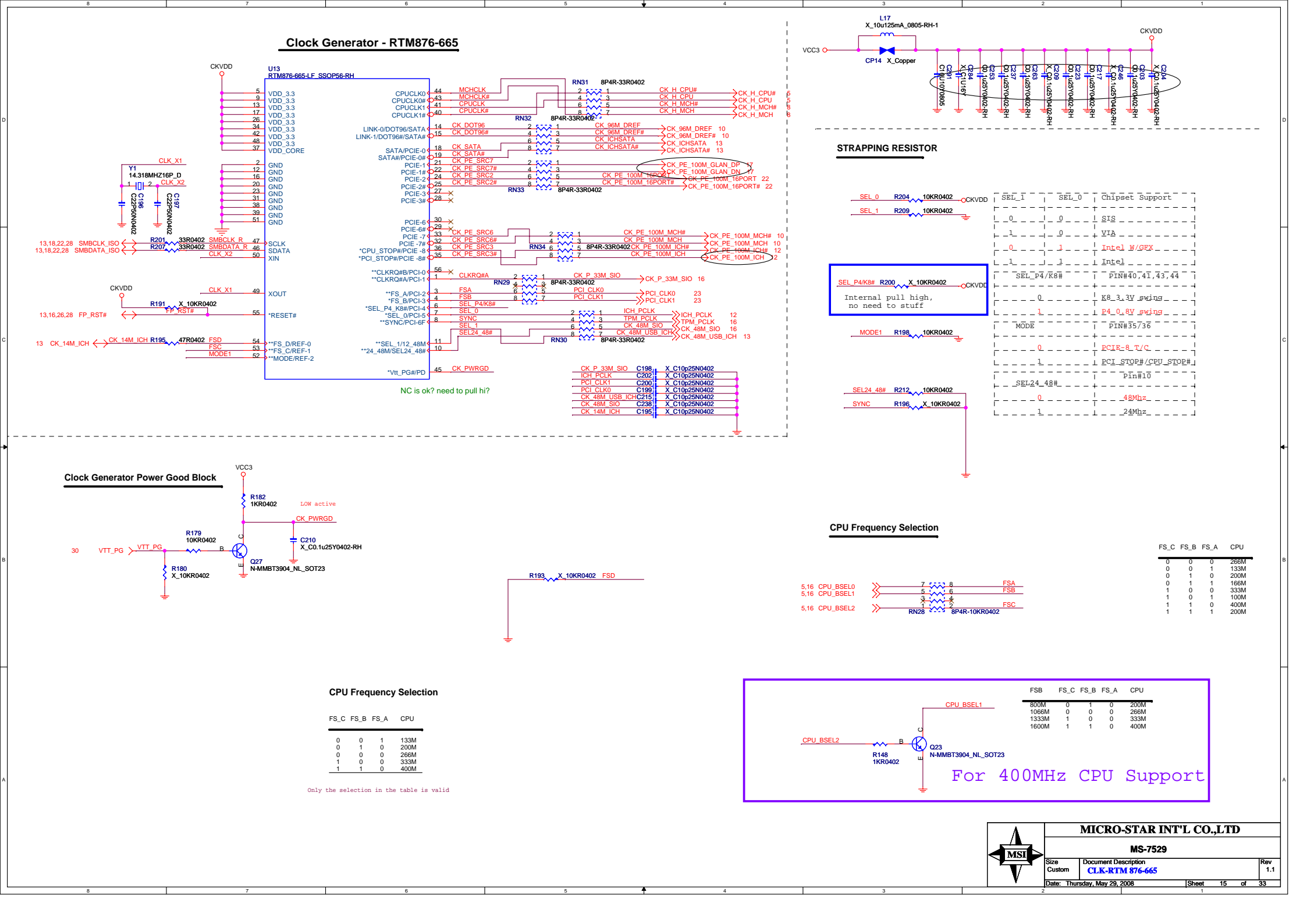
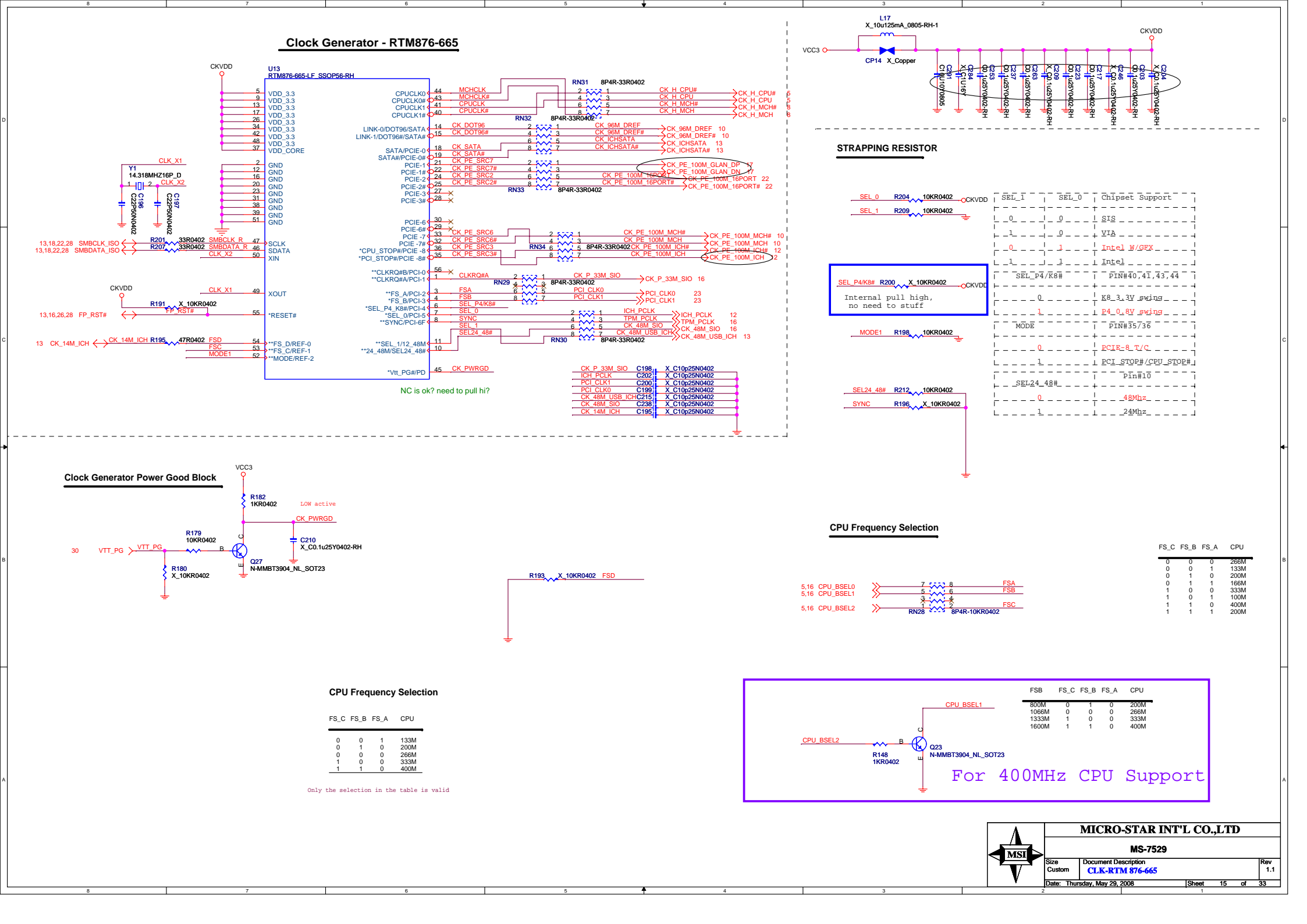
Clock Generator - RTM876-665

Clock Generator - RTM876-665

Clock Generator - RTM876-665



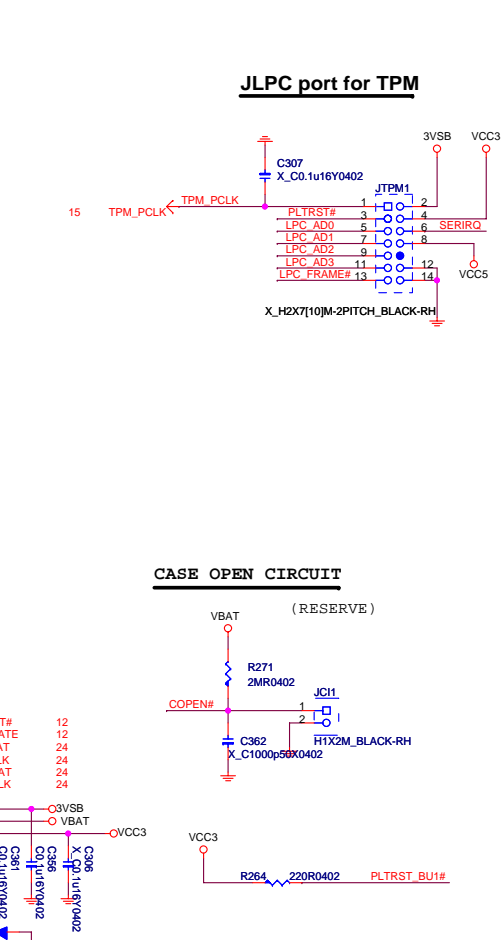
Clock Generator - RTM876-665

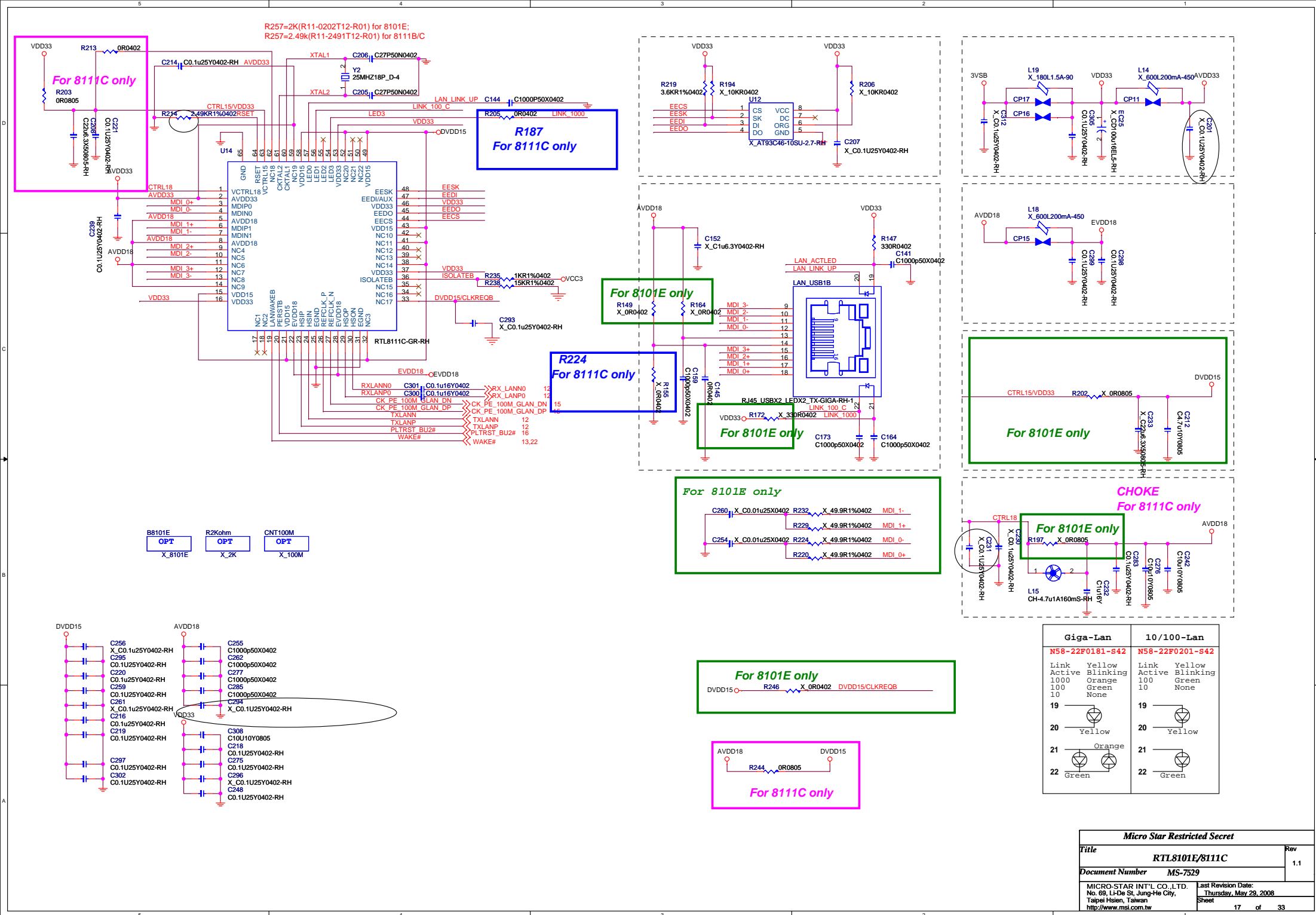


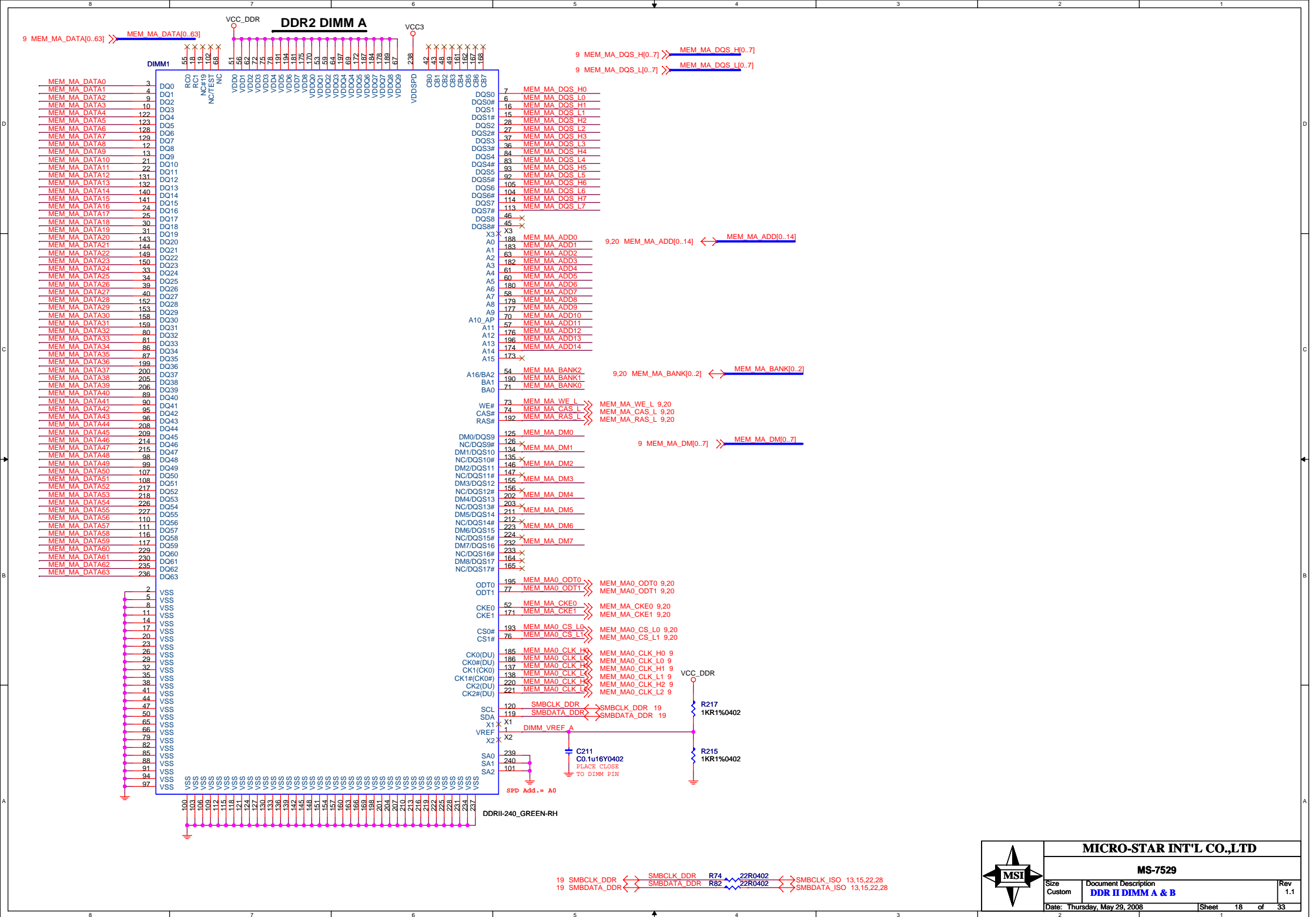
Clock Generator - RTM876-665

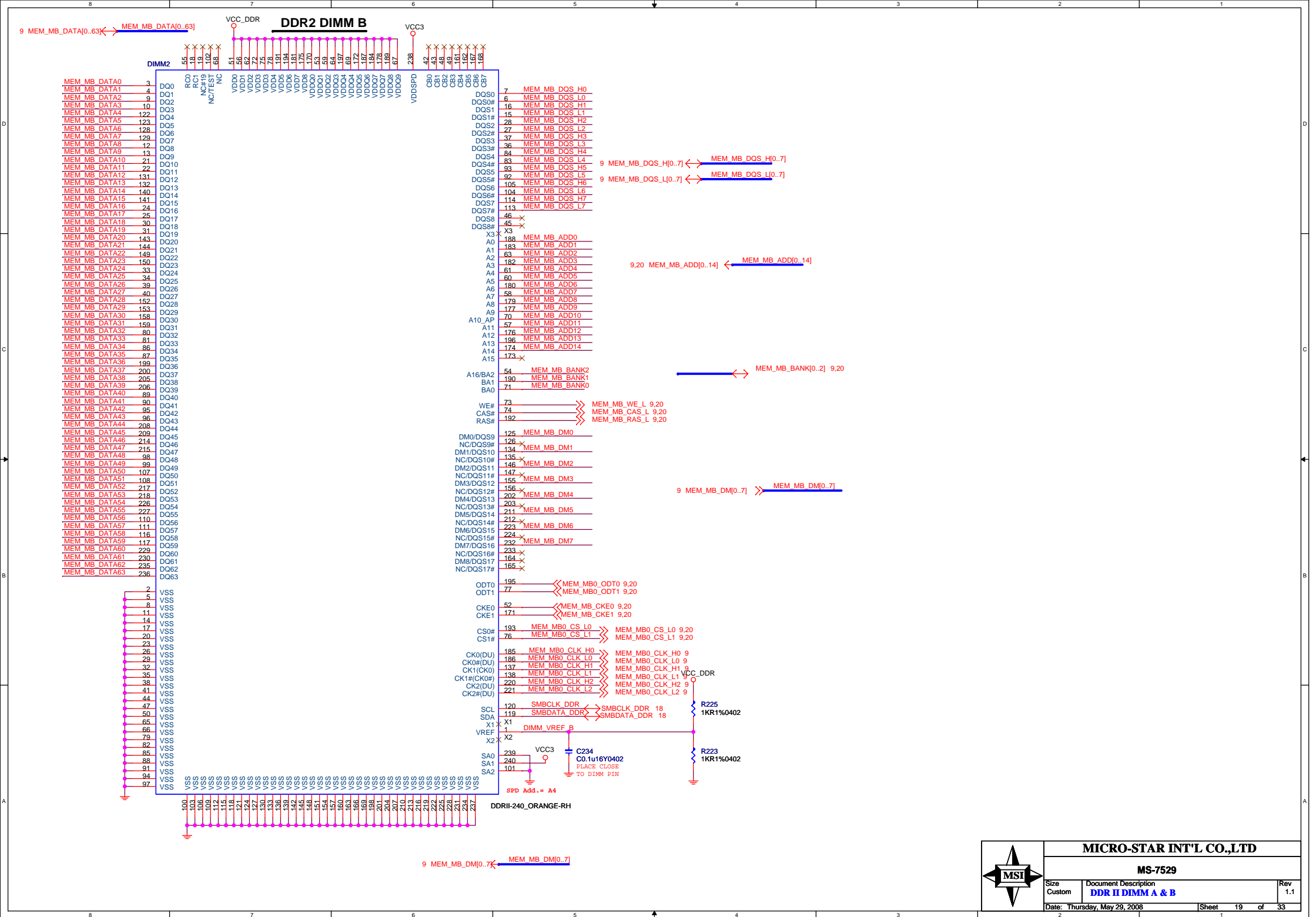
Clock Generator - RTM876-665

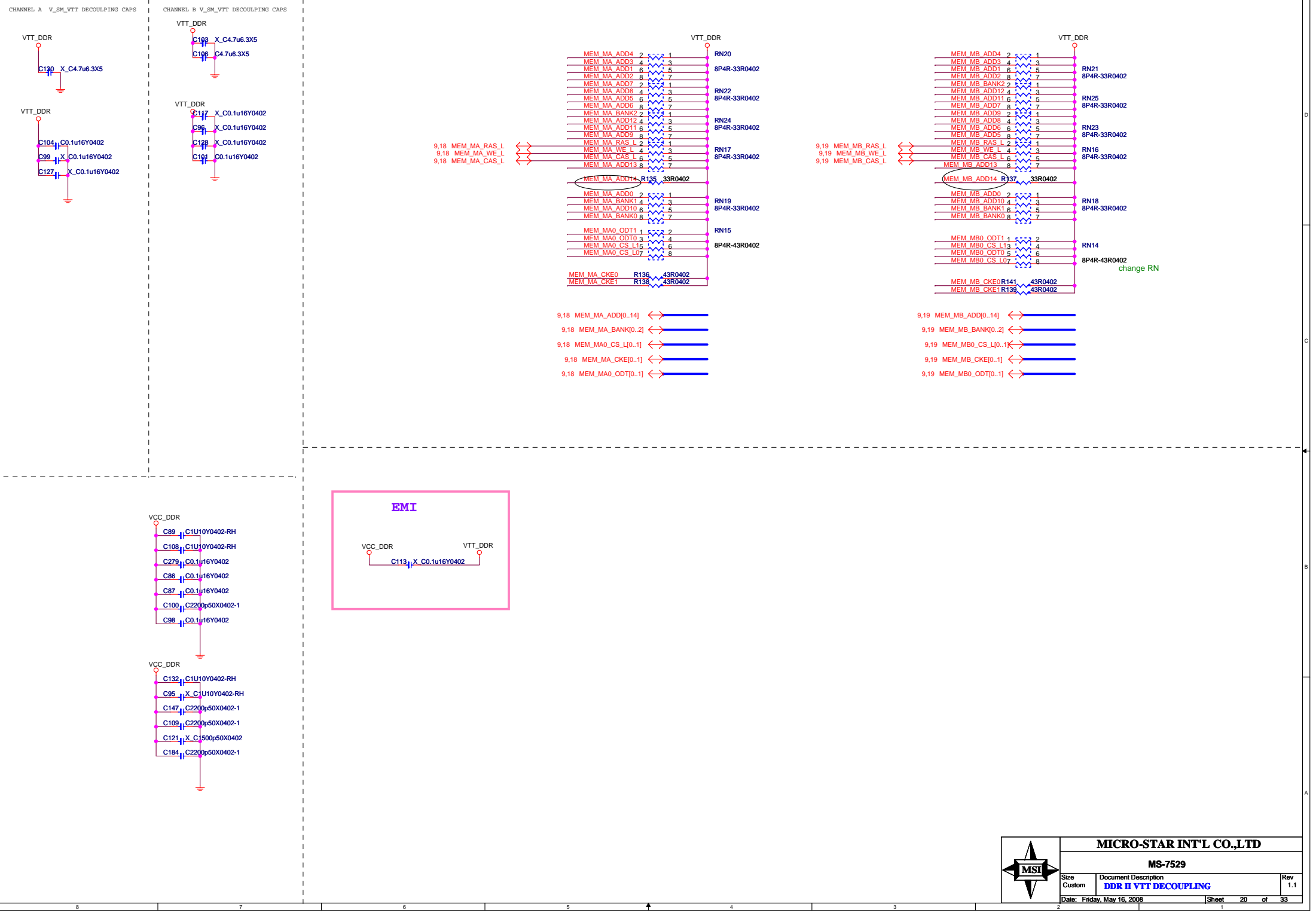
Clock Generator - RTM876-665



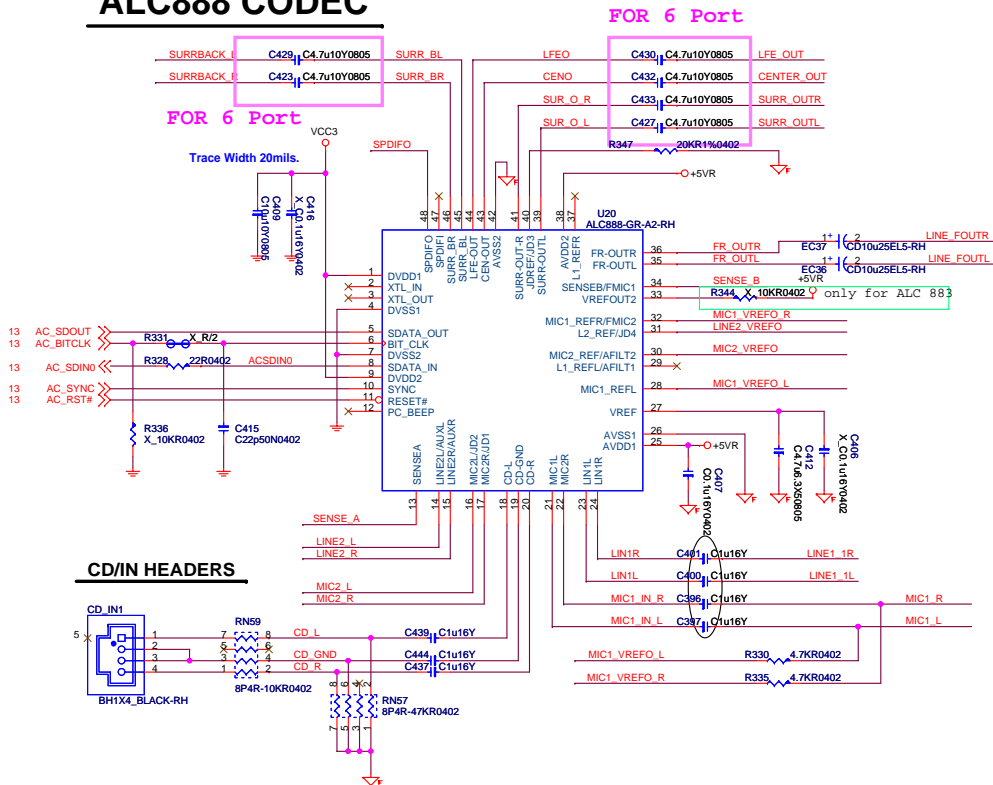




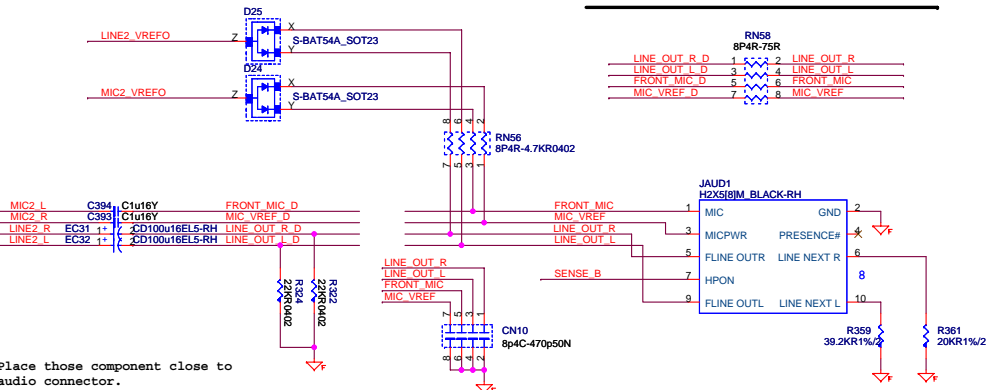




ALC888 CODEC

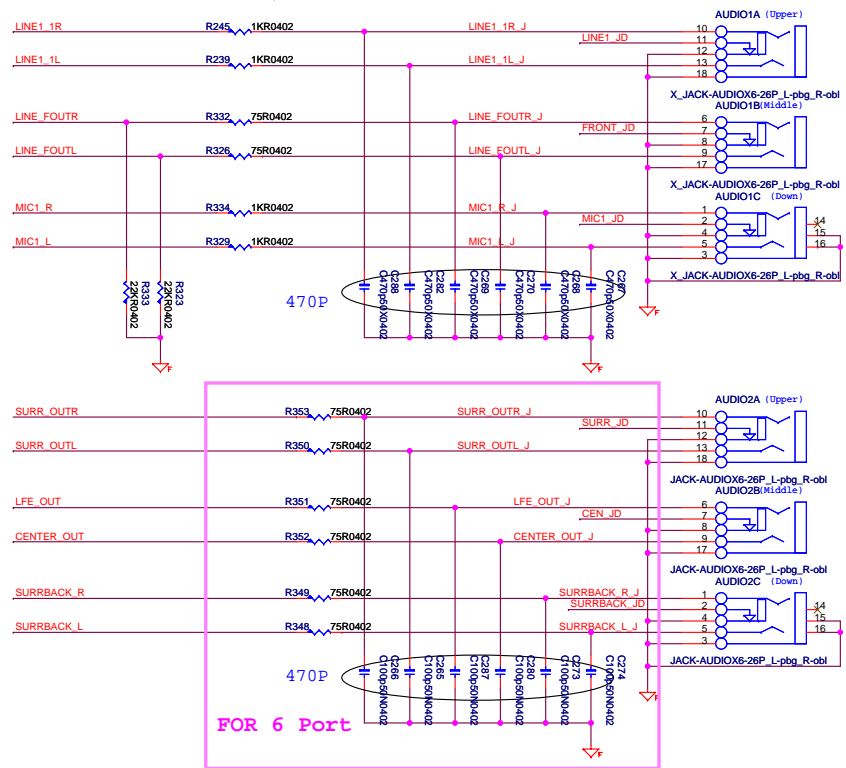


Azalia Front Audio Connector

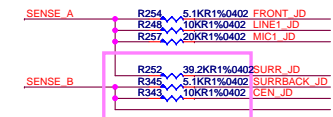


Place those component close to audio connector.

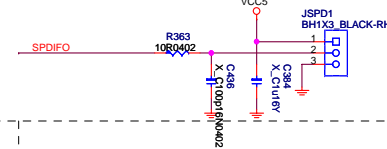
ALC888 JACK



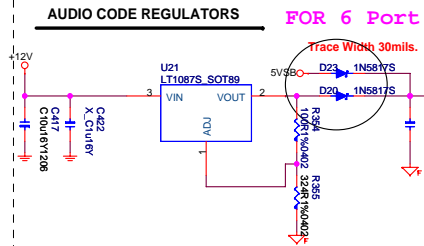
ALC883 JACK DETECT



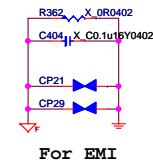
SPDIF OUT



AUDIO CODE REGULATORS



FOR 6 Port



For EMI



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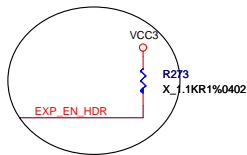
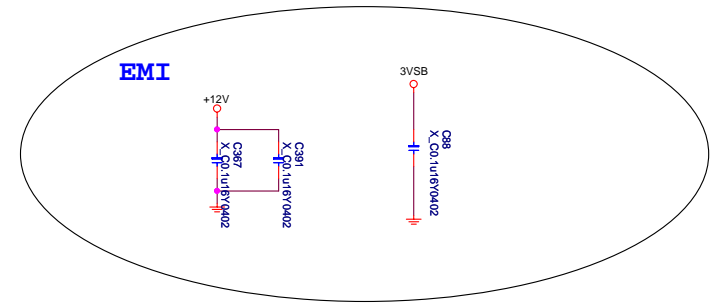
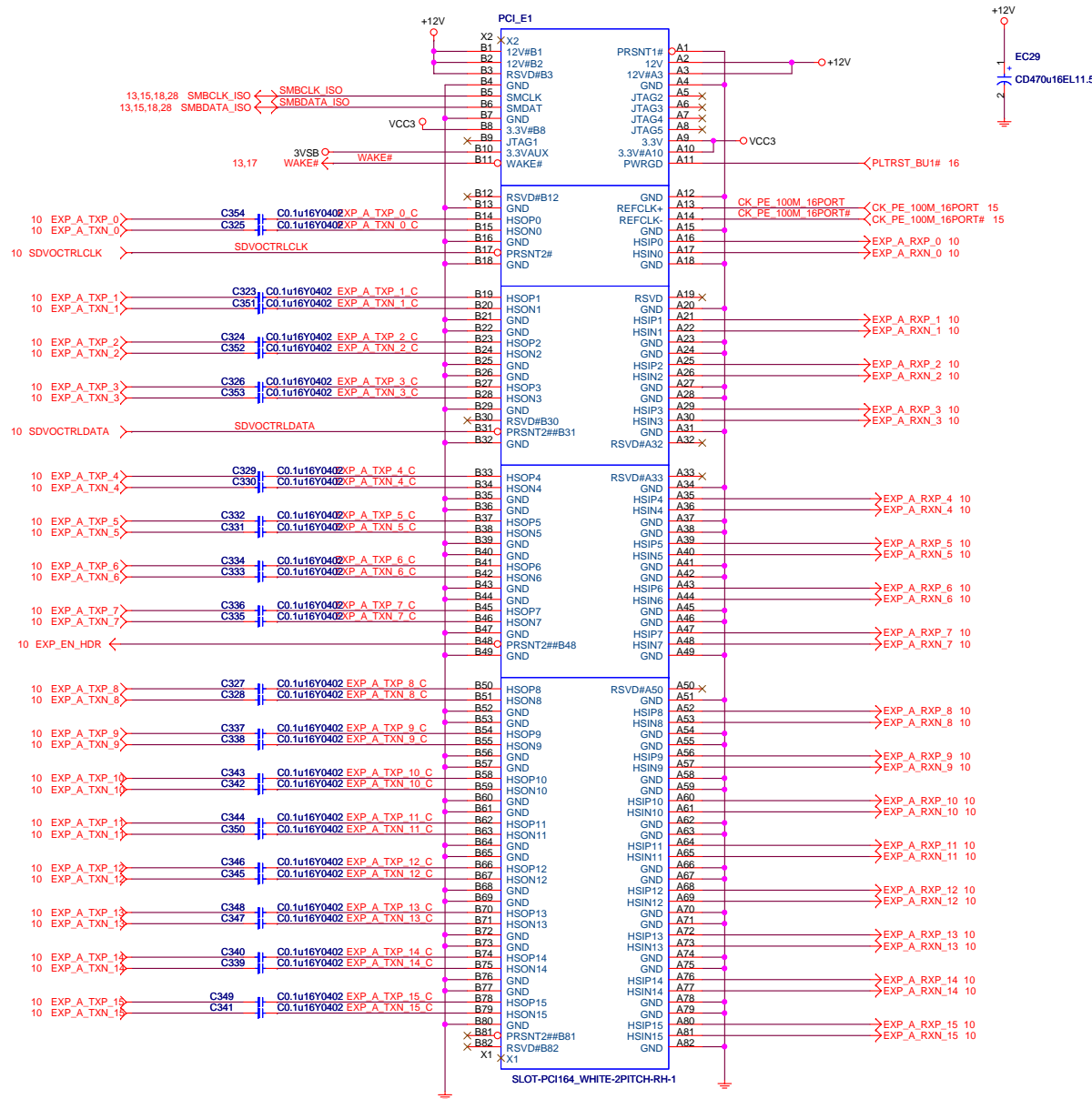
Size Custom	Document Description 21 HD ALC888
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Rev	
1.1	

Date: Thursday, May 29, 2008

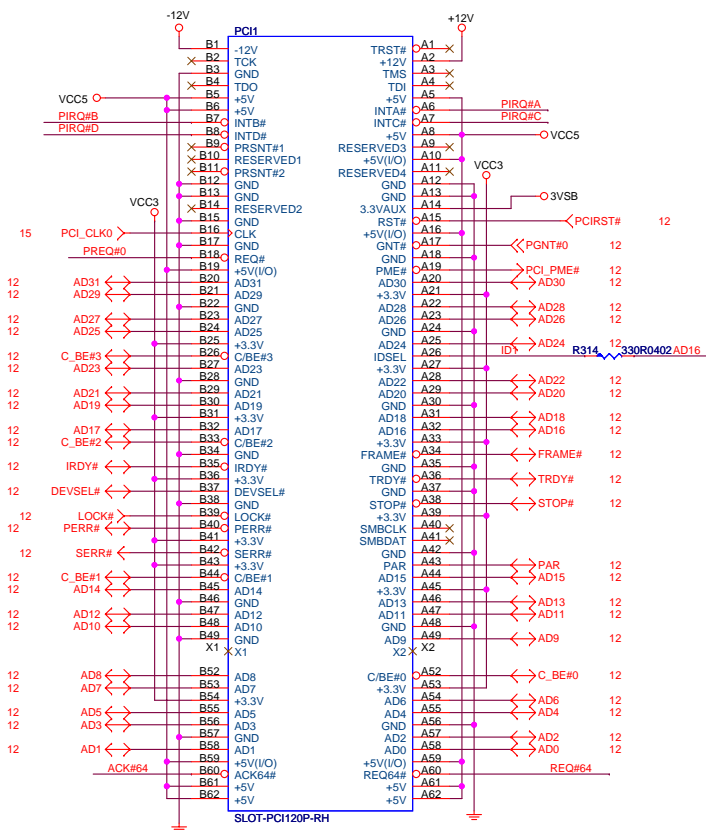
Sheet	21	of	33
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PCIe X16 PORT



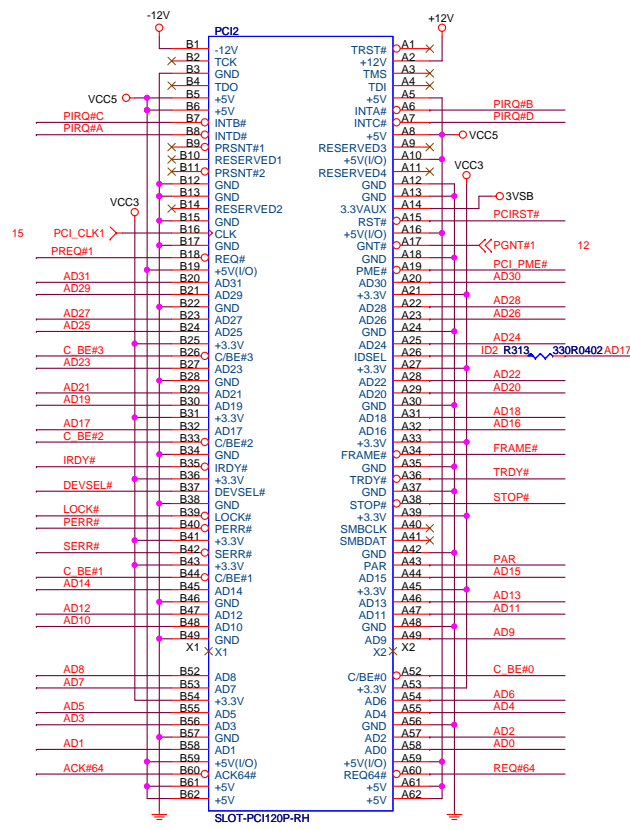
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MS-7529			
Size	Document Description	Rev	
Custom	PCI EXPRESS X16 & X1	1.1	
Date: Thursday, May 29, 2008		Sheet	22 of 33

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



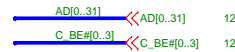
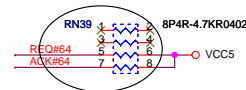
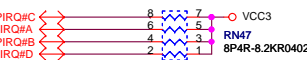
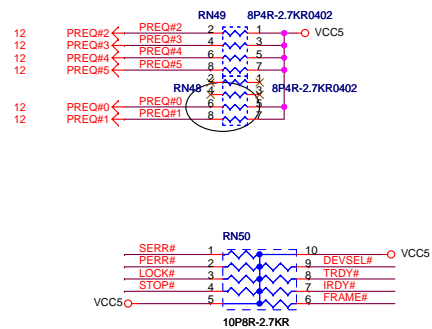
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

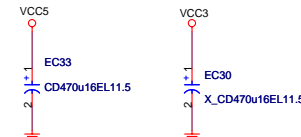


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



12 PREQ#[0..5]

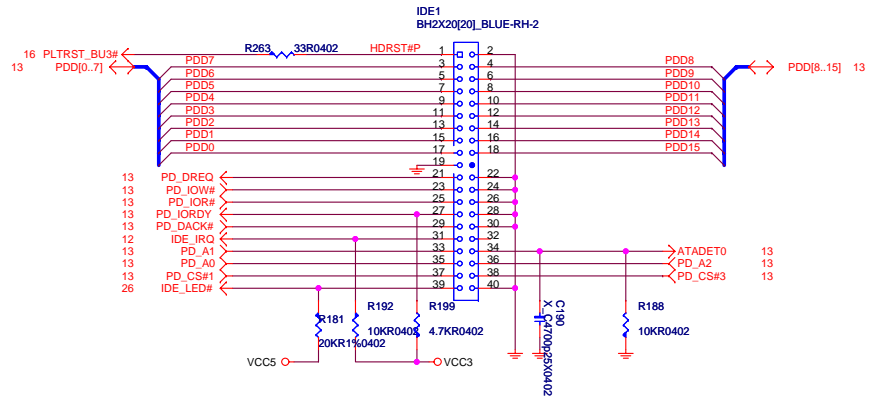


MICRO-STAR INT'L CO.,LTD

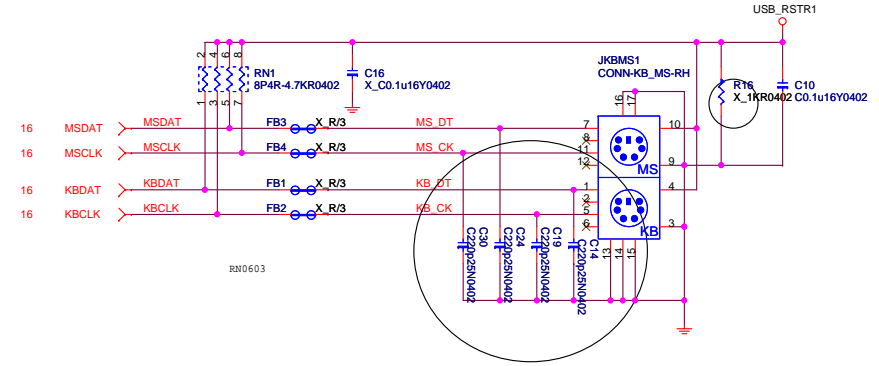
MS-7529

Size	Document Description	Rev
Custom	PCI Slot 1 & 2	1.1
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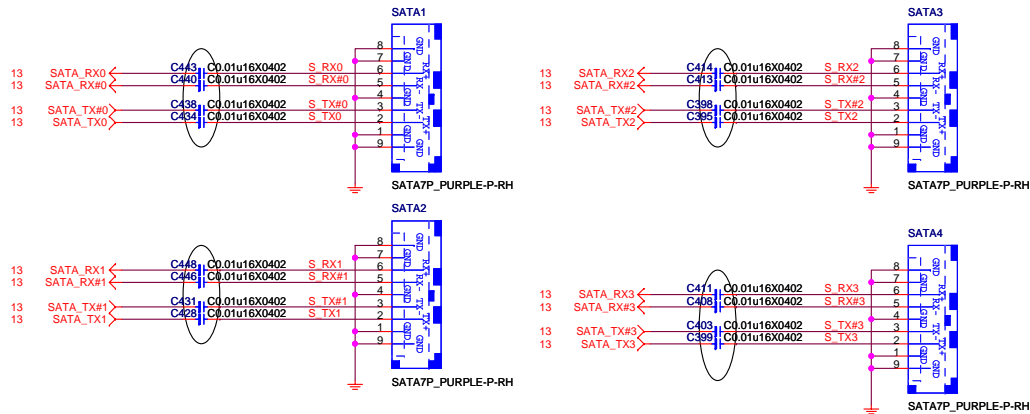
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK

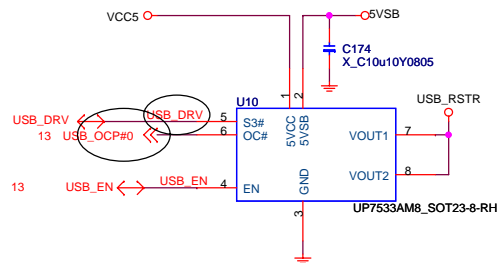


MICRO-STAR INT'L CO.,LTD

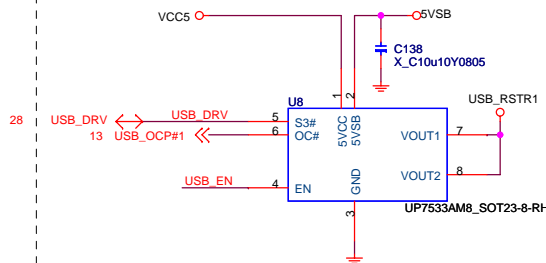
MS-7529

Size Custom	Document Description IDE & SATA Connectors	Rev 1.1
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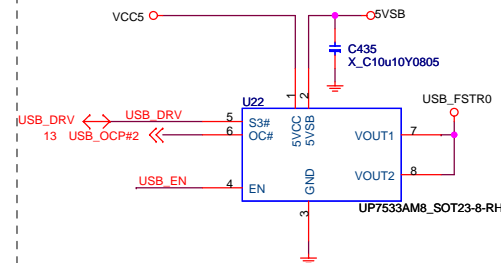
POWER CIRCUIT FOR USB PORT 0,1



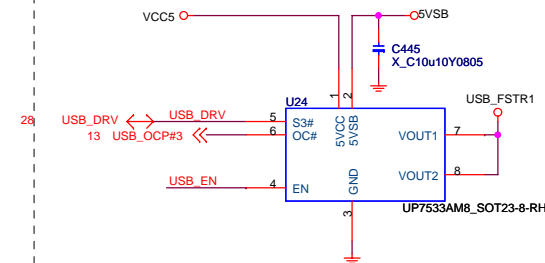
POWER CIRCUIT FOR USB PORT 2,3



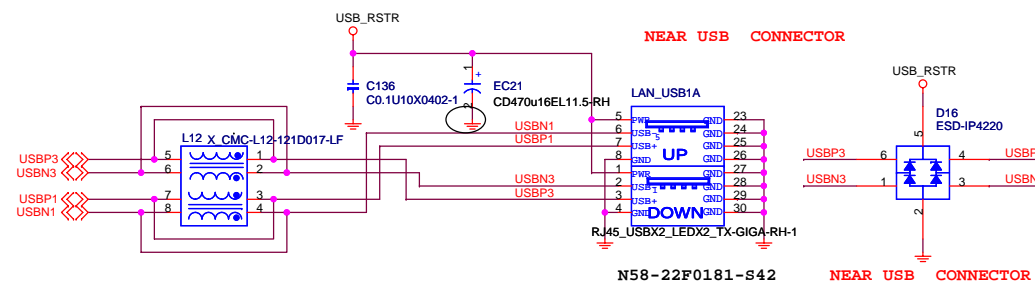
POWER CIRCUIT FOR USB PORT 4,5



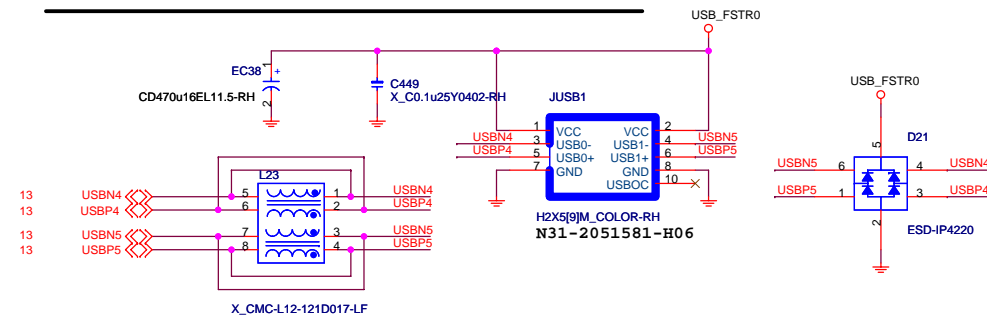
POWER CIRCUIT FOR USB PORT 6,7



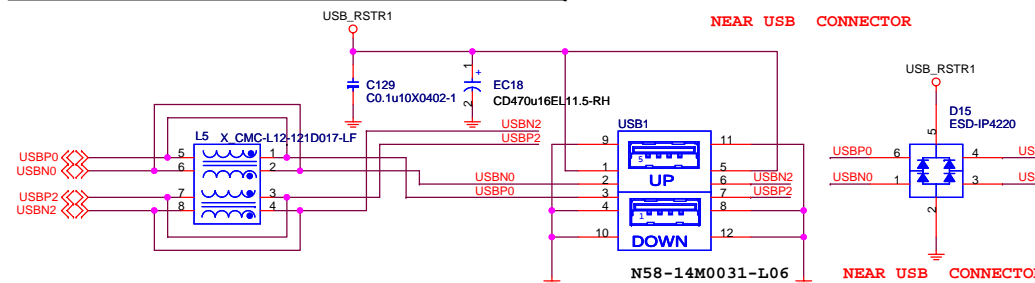
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



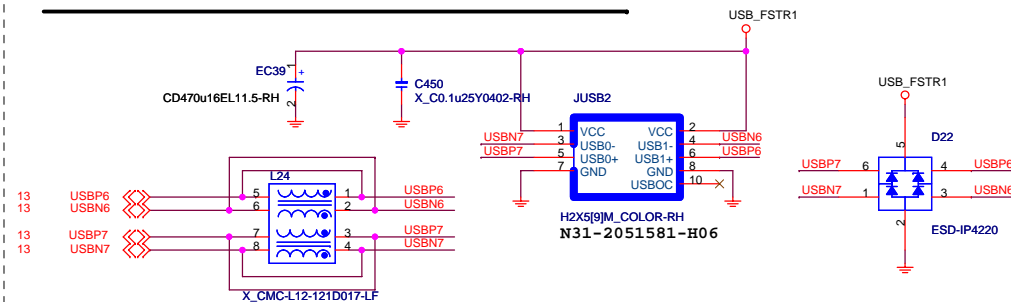
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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Custom	USB CONNECTORS	1.1
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ATX Connector

[illegible]

MSI Front Panel Connector

The diagram illustrates the wiring for the MSI Front Panel Connector. It shows a 13-pin connector with the following connections:

- Pin 1:** SUS_LED
- Pin 3:** PWR_LED
- Pin 5:** GND
- Pin 2:** SPEAKER
- Pin 4:** BUZ+
- Pin 6:** BUZ-
- Pin 8:** VCCSPK
- Pin 10:** VCC5
- Pin 11:** X
- Pin 12:** NL_SOT23
- Pin 13:** A
- Pin 14:** C
- Pin 15:** VCC5

Key components and their connections include:

- Diode D18 (BAS32L_LL34):** Connected between pins 14 and 15.
- Resistor R272 (2.2K):** Connected between pins 13 and 14.
- Resistor R277 (X 0R0402):** Connected between pins 11 and 12.
- Transistor Q33 (N-MMBT3904):** Connected between pins 10 and 11.
- Speaker:** Connected between pins 2 and 4.
- Buzzer:** Connected between pins 4 and 6.
- Ground:** Connected to pins 5 and 8.

LED (for Fintek 71882)

The schematic diagram illustrates the LED driver circuit for the Fintek F71882. The circuit is powered by a 5VSB supply. It features two NPN transistors, Q39 and Q41, both of type N-MMBT3904_NL_SOT23, which drive the SUS_LED and PWR_LED respectively. The feedback network consists of resistors RN40 (8P4R-680R0402-RH) and RN52 (8P4R-4.7KR0402). The circuit is connected to a 5VSB input, and the output is connected to the SUS_LED and PWR_LED. The 8P4R-680R0402-RH and 8P4R-4.7KR0402 components are also shown.

CPU FAN

16 CPU-FAN_CTL

16

SYSTEM FAN

The schematic diagram illustrates the electrical connection for the SYSTEM FAN. A +12V supply is connected to a network of resistors and a fan. The circuit is divided into two sections by a dashed line: 'SYSTEM FAN' and 'FAN'.

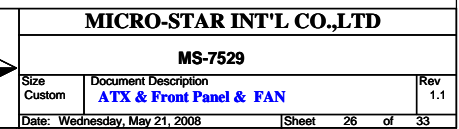
Components and Connections:

- +12V Supply:** Connected to the top of the circuit.
- R41 (4.7K R0402):** A resistor connected between the +12V supply and the top of the fan.
- R48 (27K R0402):** A resistor connected between the top of the fan and the output line.
- R54 (10K R0402):** A resistor connected between the output line and ground.
- C11 (X_C10u16X51206-RH):** The fan component, labeled 'H1X3B-FR-WHITE-RH'. It has four pins: 1 (ground), 2 (ground), 3 (top of fan), and 4 (top of fan).
- Output:** The output line is labeled 'SYS_FAN1' with a red arrow and the number '16'.

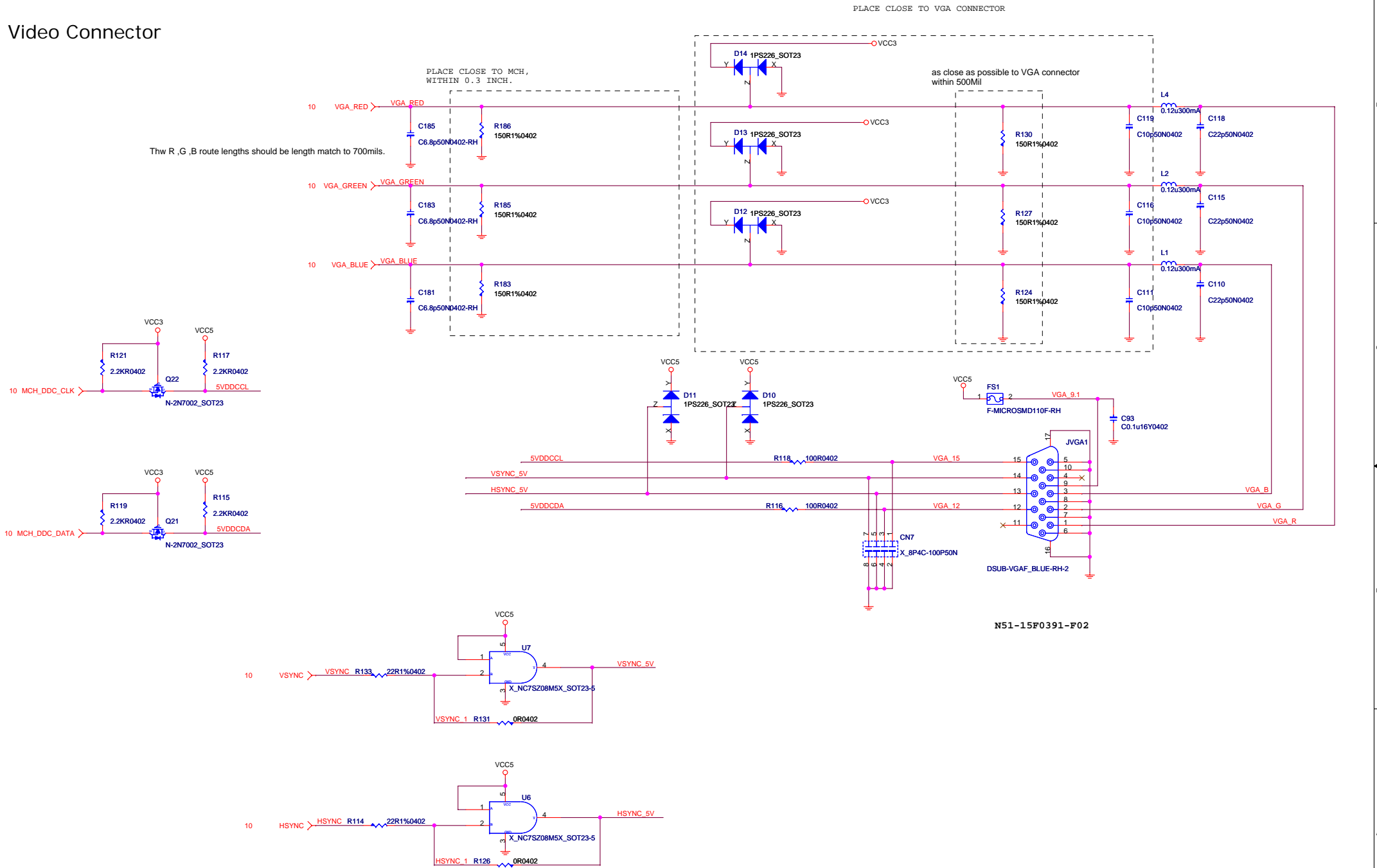
PWR_FAN

The schematic diagram illustrates the PWR_FAN circuit. It features a +12V power supply connected to a network of resistors and a capacitor. The circuit includes a fan (SYSFAN1) and a signal output (SYS_FAN2).

- Power Supply:** +12V
- Resistors:**
 - R61: 4.7KΩ0402
 - R62: 27KΩ0402
 - R67: 10KΩ0402
- Capacitor:** C49: X_C10u16X51206-RH
- Fan:** SYSFAN1 (AH1X3B-FR_WHITE-RH)
- Signal Output:** SYS_FAN2



Video Connector

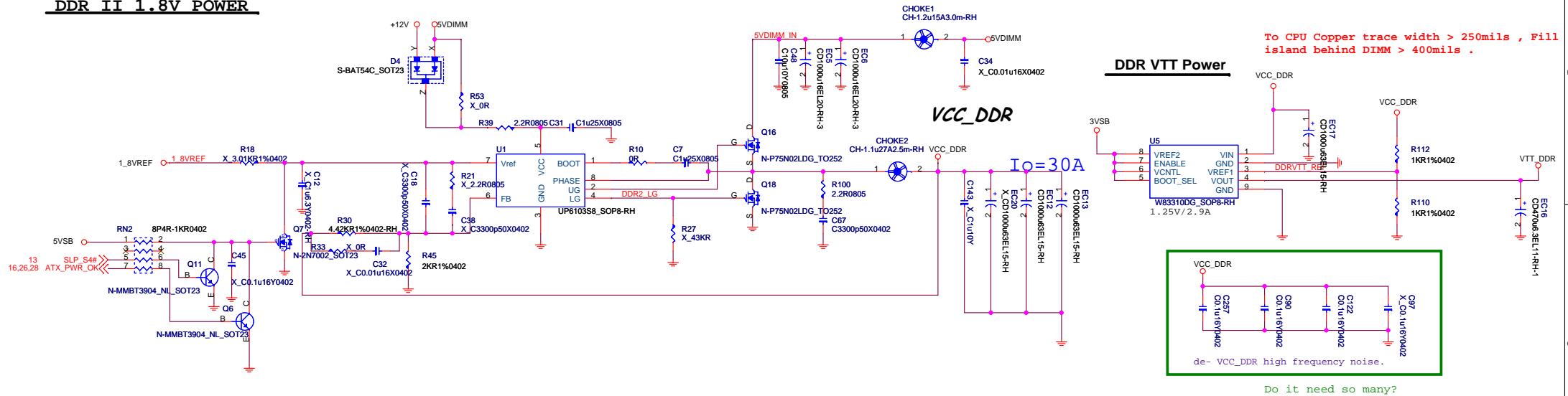


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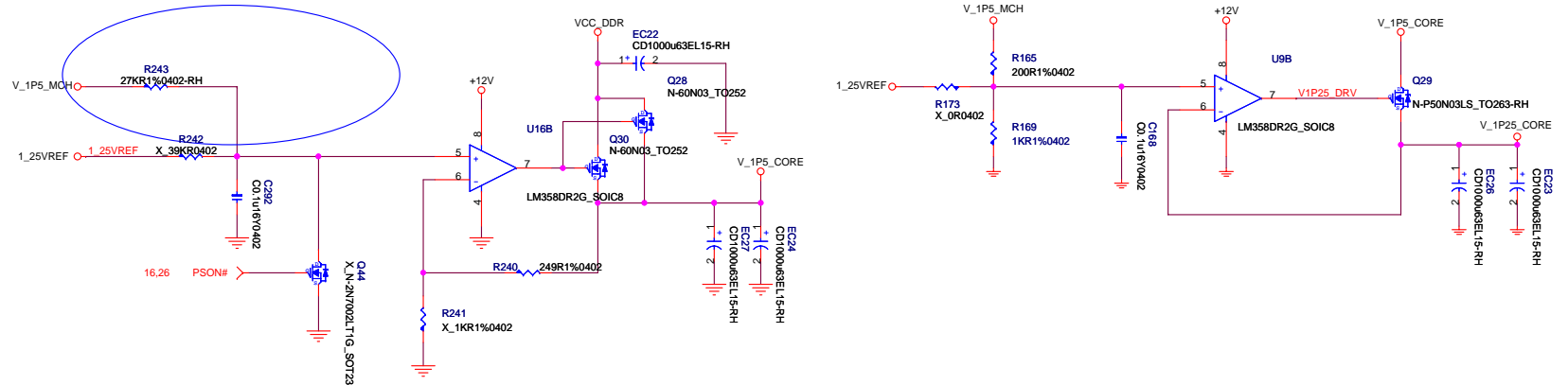
Size Custom	Document Description VGA Connector	Rev 1.1
Date: Friday, May 16, 2008		Sheet 27 of 33

DDR II 1.8V POWER

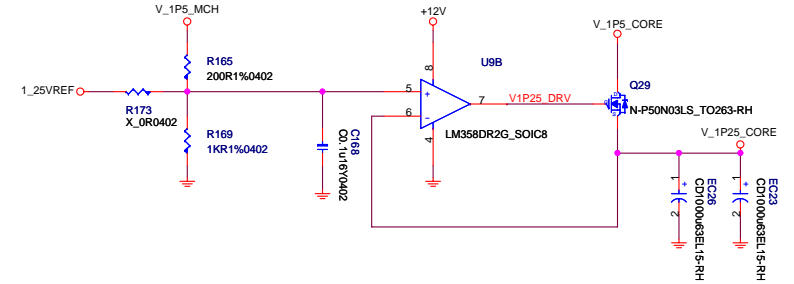


1.5V Core

For cost down



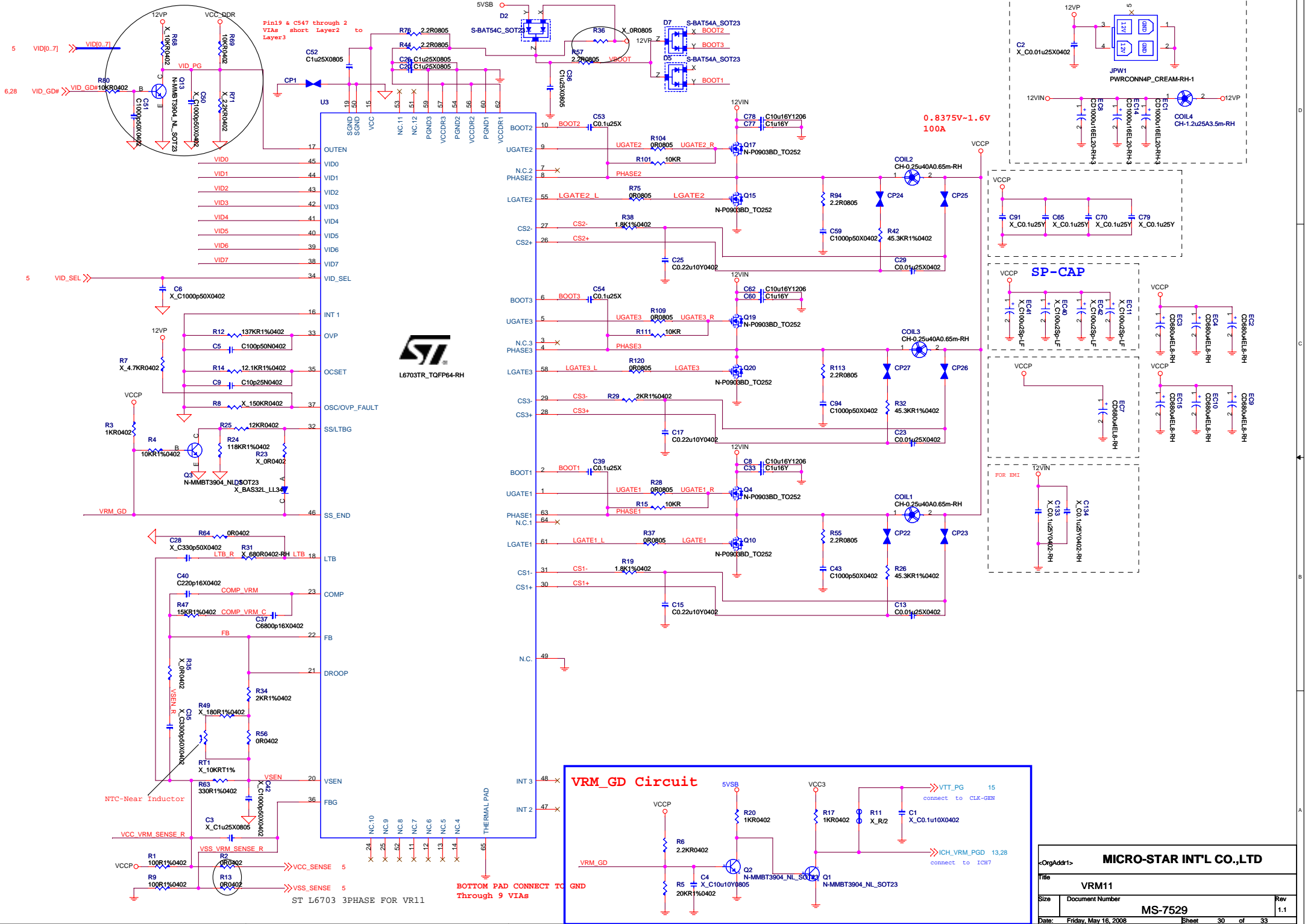
V_1P25_CORE 18.1A+2.47A+2.94A



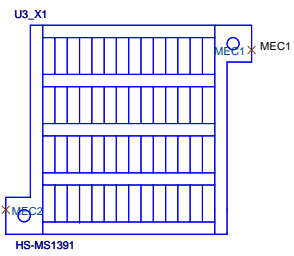
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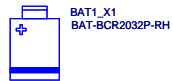
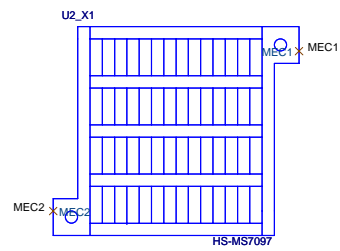
Size Custom	Document Description NB Core Power & DDR Power	Rev 1.1
Date: Tuesday, June 03, 2008	Sheet 29 of 33	



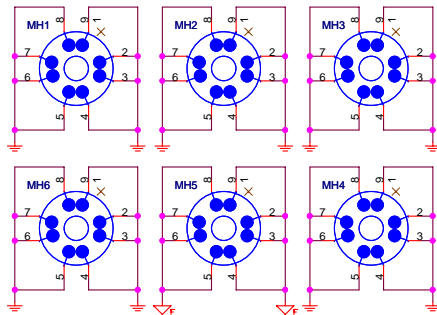
ICH7 HEATSINK



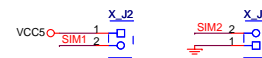
MCH HEATSINK



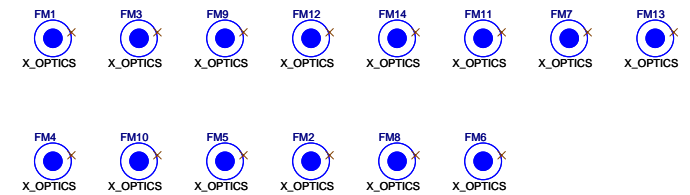
Mounting Holes



Simulation



Optics Orientation Holes



ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPIO3(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.									

SIO Fintek71882FG(CONTINUE)					
GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82		INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICES		MCP1 INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A		PREQ#0 PGNT#0	AD16	PCI_CLK0
	PIRQ#B				
	PIRQ#C				
	PIRQ#D				
PCI2	PIRQ#B		PREQ#1 PGNT#1	AD17	PCI_CLK1
	PIRQ#C				
	PIRQ#D				
	PIRQ#A				

JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A
		P_DDR1_A/N_DDR1_A
		P_DDR2_A/N_DDR2_A
		P_DDR0_B/N_DDR0_B
DIMM B	A4H	P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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0A Change list:

- 1. Add DMI Audio net name
- 2. Change LED Power pull high to 680 Change r20 to 1.5K
- 3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
- 4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
- 5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
- 6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
- 7. Add 5VCC TO 3VCC sequence
- 8. change TESTPIN30 to TPC20B
- 9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
- 10. Modify V_1P25_CORE to G31

1.0 Change list:

- 1. U11 EN(pin3)change to USB_DRV
- 2. Add SIO pin55 SKTOCC# pull up to 3vsb
- 3. Swap RN26
- 4. add Control UP7501 power sequence

Title			
History			
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